SIGNAL PROCESSING FOR ARCAS FALLING SPHERE PROGRAM

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FINAL REPORT

Period Covered: 22 May 1967 to 30 November 1968

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Project No. 6562 Task No. 668201

CONTRACT MONITOR

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Prepared for

AIR FORCE CAMBRIDGE RESEARCH LABORATORIES

OFFICE OF AEROSPACE RESEARCH

UNITED STATES AIR FORCE

BEDFORD, MASSACHUSETTS 01730

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Contract No. F19628-67-C-0218
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ABSTRACT

Under contract F19628-67-C-0218, GCA Corporation has completed the design for a rocket probe system which will determine air density at altitudes of 70 to 130 km by means of the falling sphere technique. The GCA design differs from that of similar probes presently being used for obtaining density measurements primarily in the signal processing electronics. The GCA design employs a digital processor which encodes 50 complete acceleration readings per second and generates a PCM output signal whereas previous probes have been analog in nature and have made use either of a multisubcarrier FM-FM system or a commutated single subcarrier FM-FM system.

In order to confirm the validity of the electrical design, a prototype unit has been fabricated and bench tested. Temperature tests have been performed on the prototype unit and indicates that over a 0 to +60°C temperature range, an accuracy figure of ±0.1 percent has been achieved for the signal processing electronics portion of the probe system. This represents an order of magnitude improvement in accuracy over a typical FM-FM system, thus fulfilling the initial accuracy objectives of the program.

Power for the system is supplied by an internal battery pack consisting of seven rechargeable nickel-cadmium cells which have a capacity sufficient to operate the probe system for a duration of 40 minutes at room temperature.

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SECTION I

INTRODUCTION

At the present time, several methods have been used to make upper atmosphere density measurements at altitudes of 70 to 130 km. One of these utilizes an inflatable sphere which is launched by Sparrow Arcus rocket to an altitude of about 150 km. During the final portion of its ascent, the sphere is ejected, then inflated and allowed to fall freely back into the atmosphere. Three accelerometers in triaxial configuration are contained within a strut positioned across a diameter and are used to measure the deceleration forces encountered as the sphere enters the atmosphere. At the same time, the velocity of the sphere is measured using radar skin tracking. A commutated FM telemetry link is used to transmit the data from the triaxial accelerometer to a ground station. Atmospheric density is derived indirectly from the above by inserting the measured values of velocity and acceleration in the drag equation and using values of drag coefficients determined from wind tunnel tests.

The system developed by GCA Corporation under contract represents a refinement of the falling sphere rocket probe system described above. The major design departure in the system electronics from the existing system is the substitution of digital processing in place of the analog commutated FM telemetry system. The use of a digital system makes possible the achievement of approximately an order of magnitude improvement in system accuracy, and provides sufficient resolution to permit a substantial increase in the altitude regime which can be examined by a single probe.

The payload mechanical system which is used for the instrumented inflatable sphere is similar to the system which was designed under a previous contract A19628-5122. Several modifications were made which reduced cost and simplified manufacturing. Essentially the payload system consists of a split nose cone and an explosive bolt release mechanism. Bolt fragments are completely contained and cannot affect the sphere. Overall weight of the entire payload is less than 14 pounds.

SECTION II

SYSTEM SPECIFICATIONS AND PHYSICAL CHARACTERISTICS

The physical configuration of the prototype payload portion of the rocket probe system (with the mylar sphere removed) is illustrated by the photograph of Figure 1. The locations and outline shapes of the various subassemblies are indicated by the arrows in the figure. Figures 2 and 3 are photographs taken of the two major subassemblies with the outer shells removed. Power and weight breakdowns for the payload elements are summarized in Table 1. Except for the power requirement of the RCA S 170 transmitter, the power requirements and weights of each subassembly appears to be moderately well apportioned to the task performed.

The prototype model of the rocket probe system and its telemetry readout equipment has been designed to sense, encode and telemeter acceleration measurements to a ground station using the digital encoding method described in detail in Section III. The system has been tested under the required 0 + 60°C temperature environment and has been found to perform satisfactorily.

Using three mutually orthogonal linear accelerometers (Systron Donner model 4311), the system is designed to sense accelerations in the range of -1 g to +1 g. During in-flight operation the accelerometer outputs are sequentially sampled and for each accelerometer output, a serial digital signal is generated having an accuracy of about $\pm$0.1 percent and a resolution of 14 binary bits. The digital output for each accelerometer together with a unique 5-bit synchronizing code prefix and a single bit flag code is telemetered to a ground station.

Initially, the maximum sampling rate for the encoding of the analog outputs of the accelerometers was limited by the technical approach to eight acceleration readouts per second. However, as a result of the use of a successive approximation method of analog to digital conversion technique in place of the counting scheme originally contemplated, it was possible to increase the sampling rate to 50 acceleration readouts per second (150 conversions/sec).

The telemetry system consists of an RCA S 170 FM transmitter operating at 1680 MHz and delivering approximagely 150 mW to a quadraloop antenna system.

The modulation scheme consists of first frequency modulating a 70 kHz subcarrier oscillator with the serial digital output signal described above. The modulated output of the 70 kHz subcarrier oscillator then is used to frequency modulate the Model S 170 transmitter.

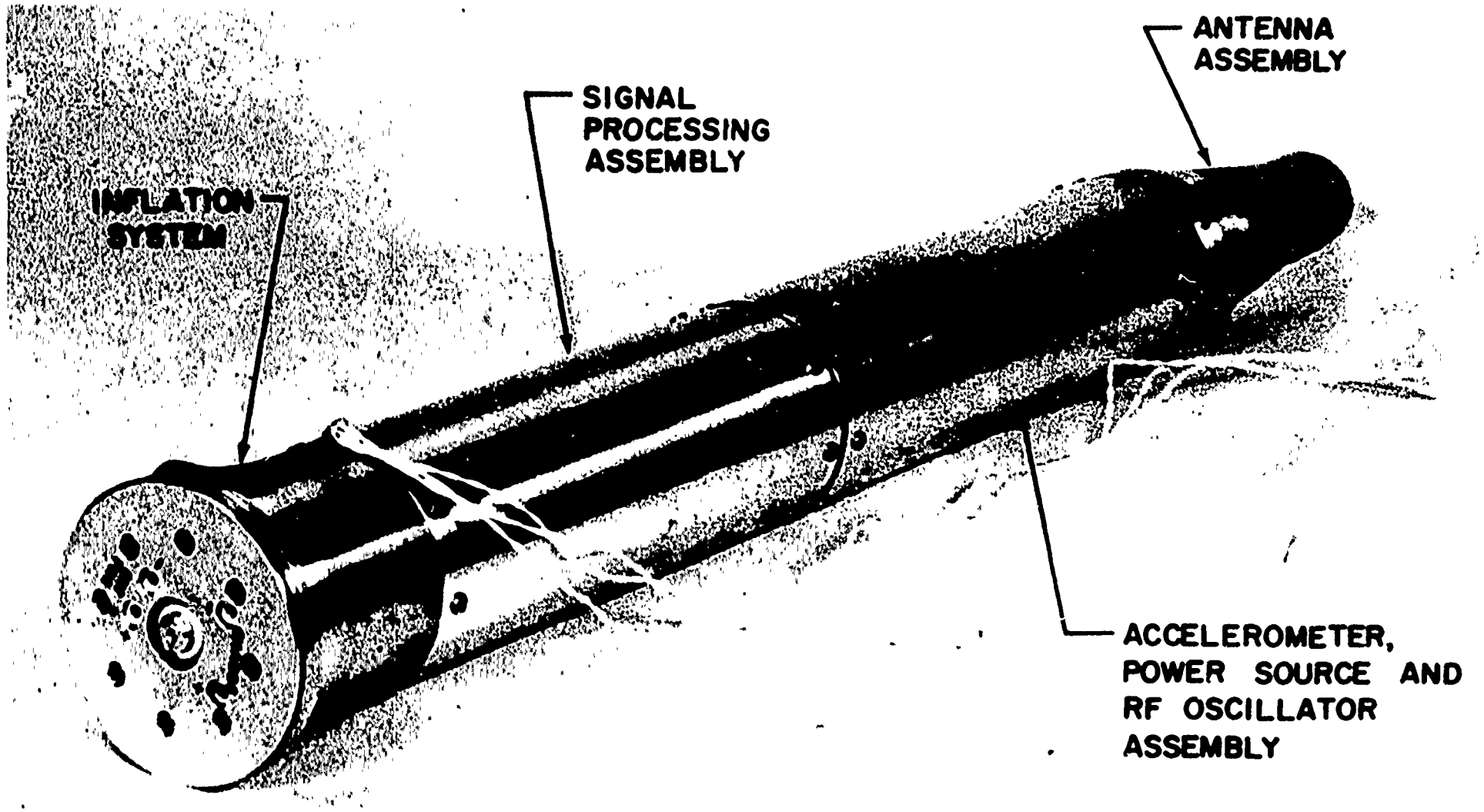


Figure 1. Photograph of prototype payload for falling sphere rocket probe system.

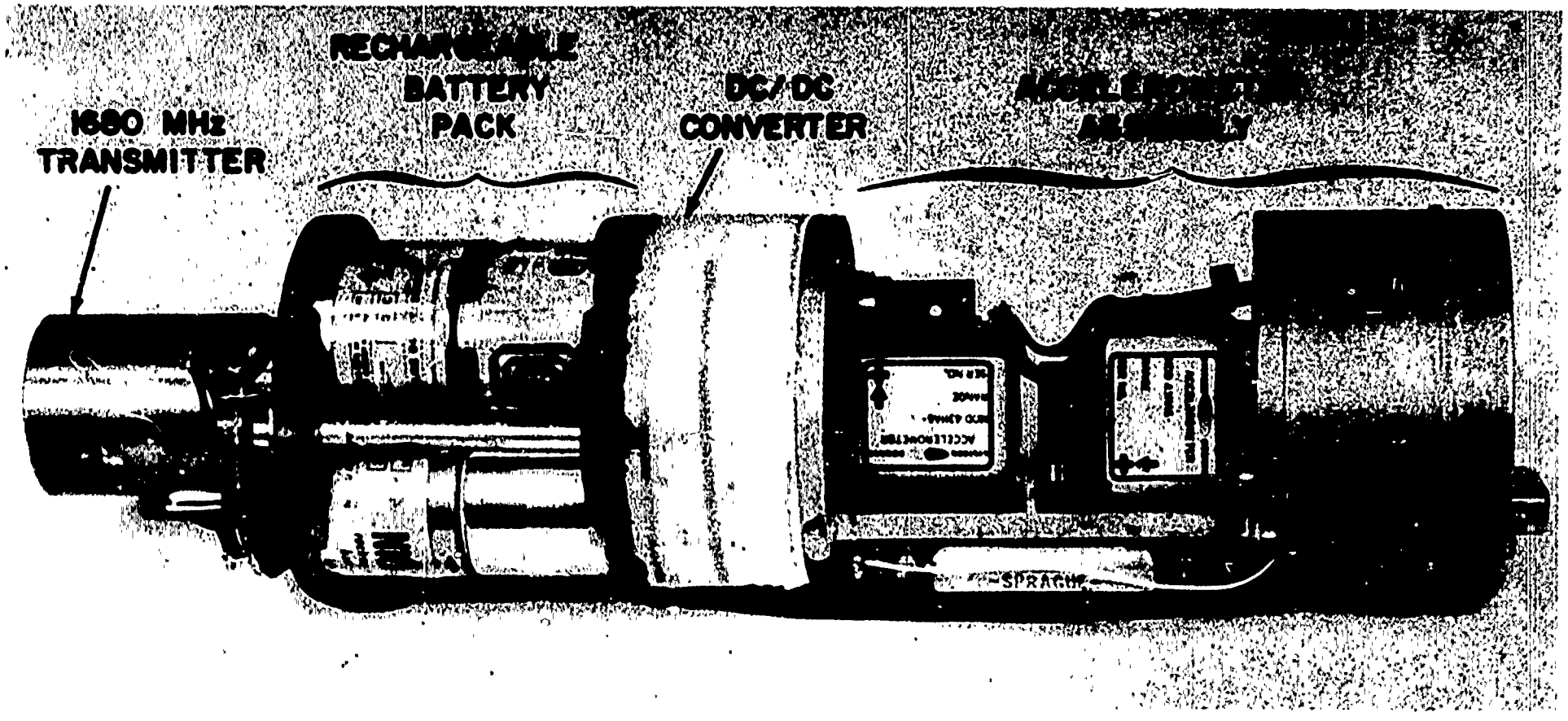


Figure 2. Accelerometer, power source and RF transmitter assembly.

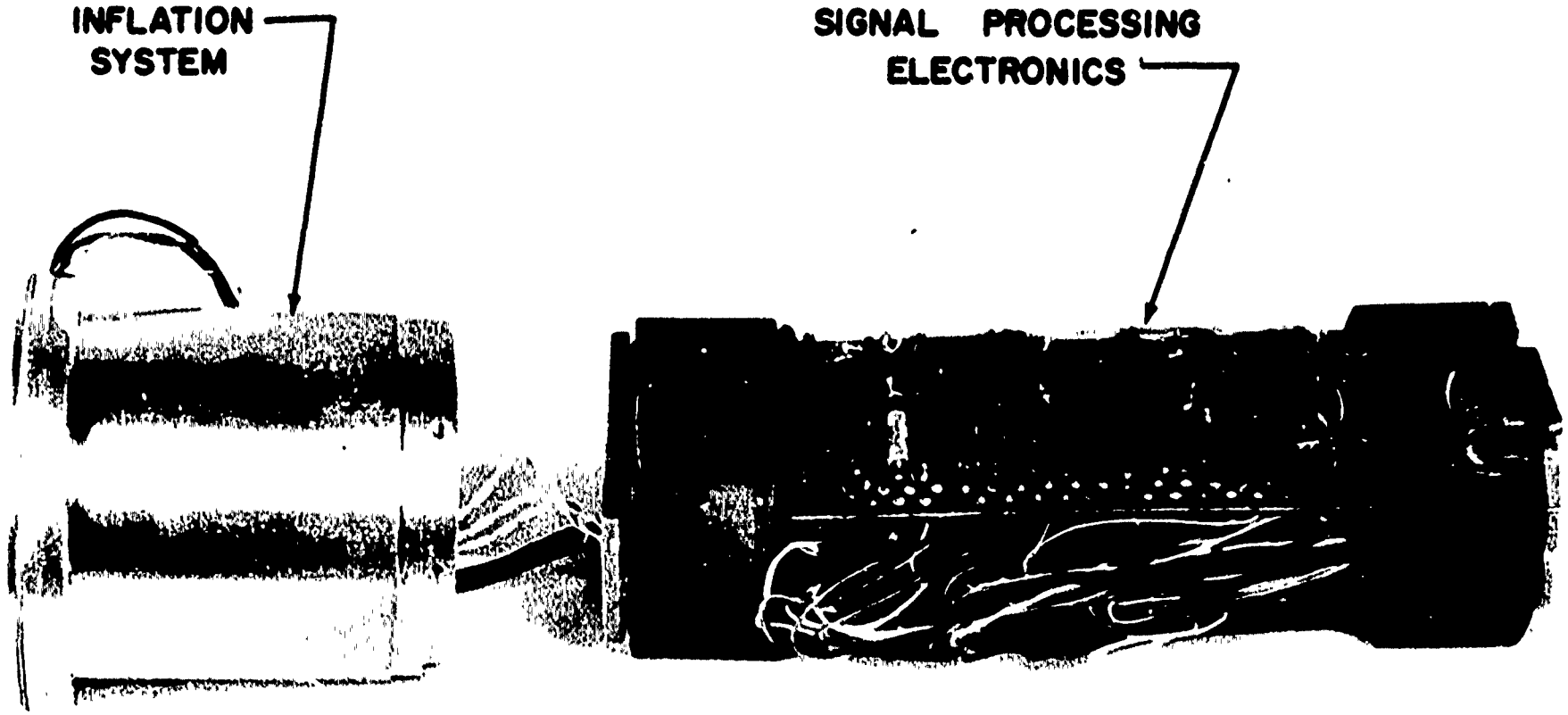


Figure 3. Inflation system and signal processing electronics.

TABLE 1

POWER AND WEIGHT BREAKDOWN OF PROTOTYPE ROCKET PROBE SYSTEM

SUBASSEMBLY	POWER CONSUMPTION	WEIGHT
Antenna assembly and RF cables	--	201 grams
Accelerometer assembly	0.45 watts at +15V 0.45 watts at -15V	821 grams
DC-to-DC Converter	Input power: 8.7 to 14.5 watts Output power: 6.16 watts	
Battery pack	Output power: 1.5 amperes at 6V to 10V	
Transmitter	3.92 watts at 28V (isolated) RF output: 0.15 watts	
Signal processing electronics	0.62 watts at +17V (unregulated +15V) 0.60 watts at -17V (unregulated -15V) 0.117 watts at 5V (isolated)	320 grams
Inflation System	--	155 grams (without isopentane fluid)
Outer shell for accelerometer assembly	--	87 grams
Outer shell for signal processing electronics	--	71 grams
Mylar balloon	--	151 grams
	Weight:	1806 grams (3.97 lb)
	Measured Weight:	3.98 lb

SECTION III

SYSTEM DESCRIPTION-(ELECTRONICS)

Figure 4 illustrates the basic physical and logical subdivisions of the electronics provided for the falling sphere experiment. The electronics circuitry is located in the strut of the sphere and its primary function is to (1) sample the analog outputs (A_x, A_y and A_z) of three accelerometers in triaxial configuration, (2) convert the sampled signals to an equivalent serial binary representation, and (3) transmit the converted signals to a ground station over an L-band telemetry link.

The signal processing circuitry is contained in four circuit boards each approximately 2 inches wide by 6 inches long. DC supply voltages for the system are provided by a dc to dc converter module 2-1/2 inches in diameter by 1-1/8 inches high. The converter is powered by seven nickel-cadmium rechargeable batteries, Gould Type 0.750 SC. The telemetry transmitter consists of an RCA Model S170V9 L-band FM transmitter.

A description of the operation of the signal processing circuitry is facilitated by making reference to Figure 5 which contains the system timing diagram and also illustrates the basic format of the telemetered data. The specifications of the data format are as follows:

A. BIT STRUCTURE

1. Rate: 3 kHz

2. Format

a. Return to zero (RZ) for sync bits

b. Non-return to zero (NRZ) for data bits

B. WORD STRUCTURE

1. Length: 20 bits

2. Rate: 150 per second

C. WORD FORMAT

1. Sync

a. Location: First 5 bits (count "0" to count "4")

b. Coding: 11101, RZ format (50 percent duty cycle)

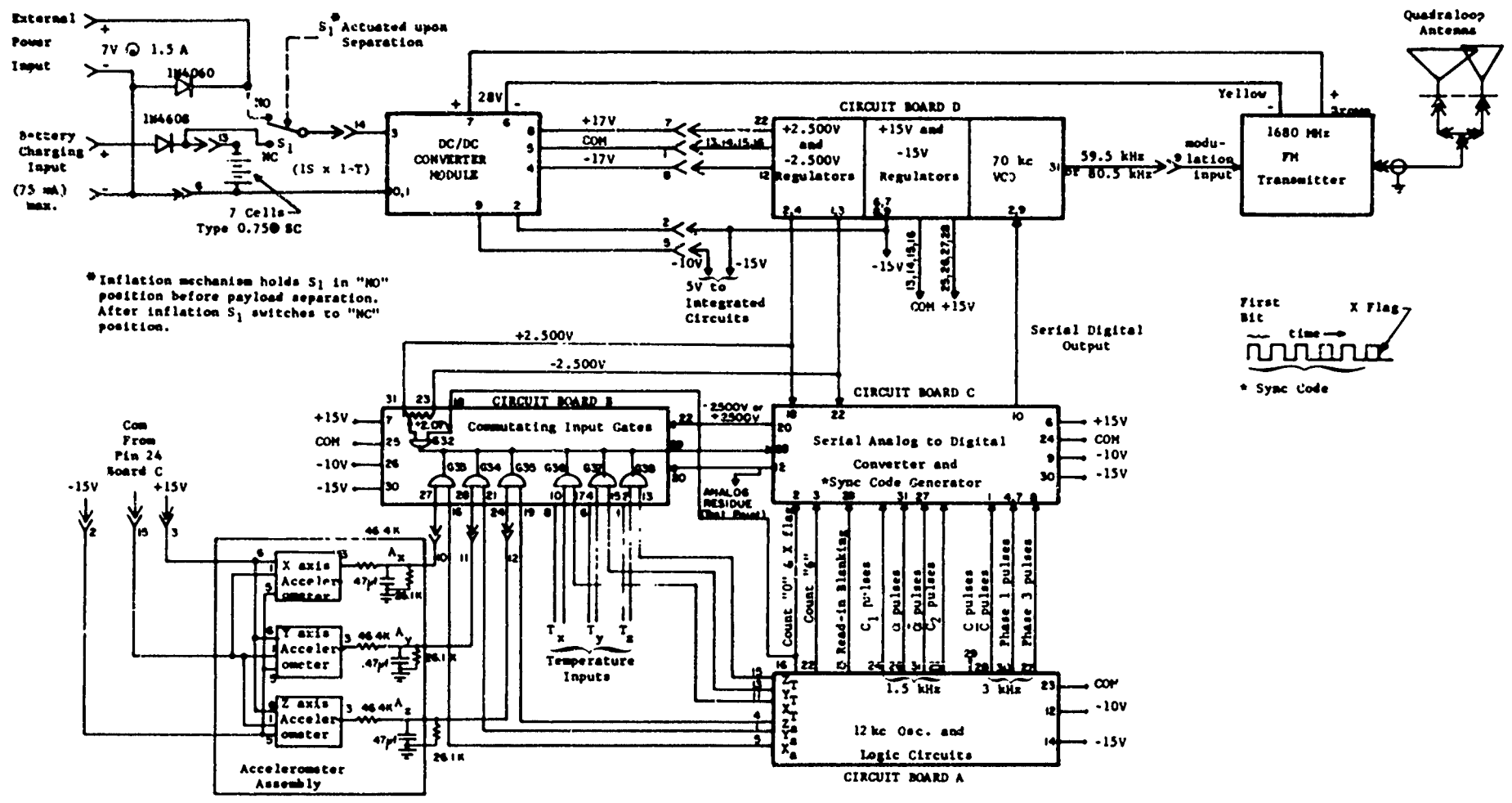


Figure 4. Block diagram falling sphere signal processing electronics.

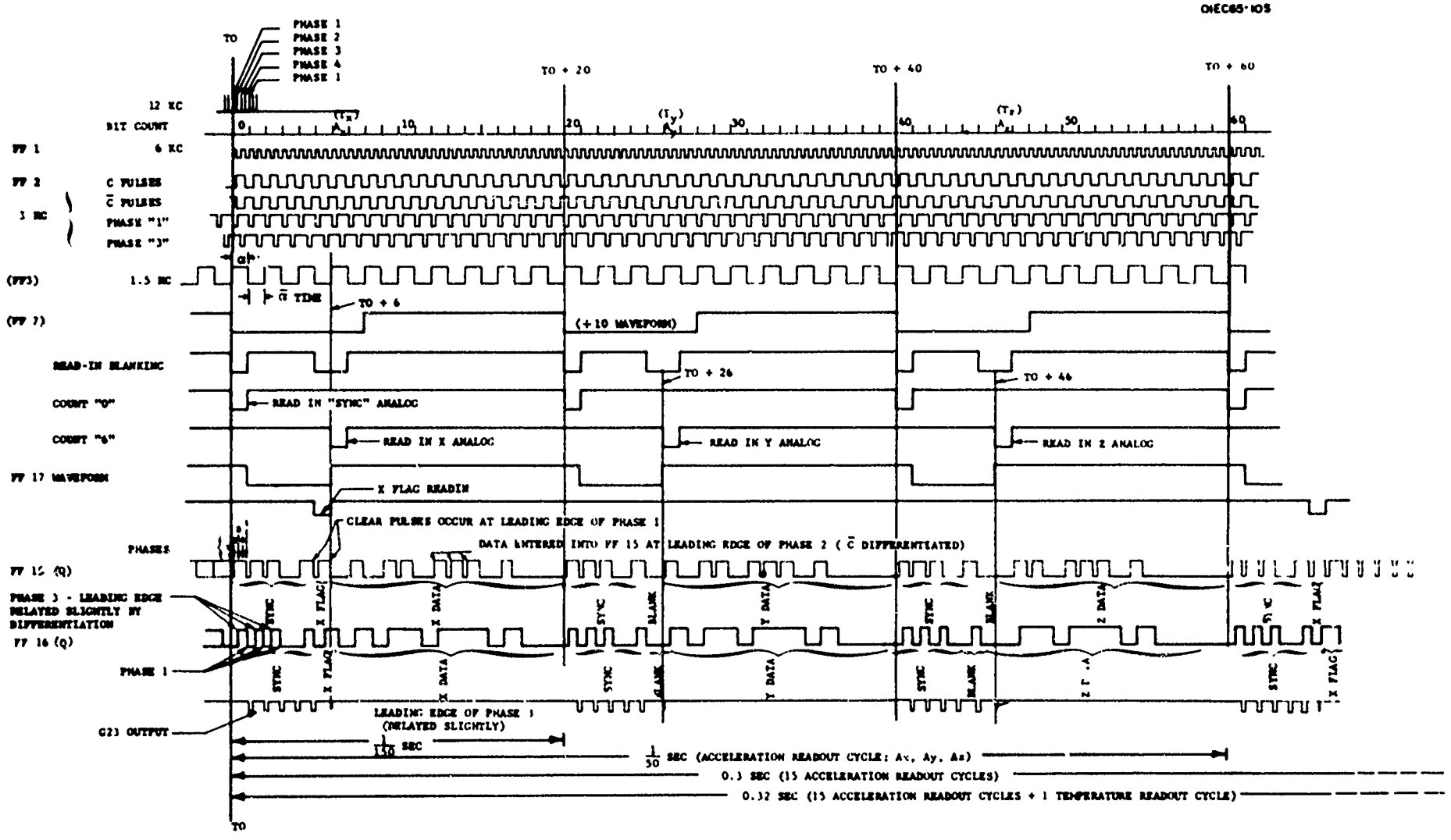


Figure 5. Timing diagram falling sphere.

2. Word Identifier (X flag)

a. Location: 6th bit (count "5")

b. Coding

(1) X flag = 0 for all words not containing X axis acceleration data

(2) X flag = 1, NRZ format for all words containing X axis acceleration data

3. Data

a. Location: Last 14 bits

b. Coding: "1"s and "0"s depending on data, NRZ format

c. Order: High order digits first

D. ACCELERATION READOUT CYCLE

1. Order: First the X axis accelerometer output, A_x, then the Y axis accelerometer output, A_y, and lastly the Z axis accelerometer output, A_z.

2. Rate: Continuously at 50 Hz rate except for every 16th readout cycle which is reserved for temperature data.

3. Axis Identifier: Flag bit at count "5" identifies A_x data.

E. TEMPERATURE READOUT CYCLE

1. Order: First T_x, then T_y and lastly T_z.

2. Rate: 3-1/8 readouts per second (substituted in place of every 16th acceleration readout cycle).

3. Identification of Temperature Readout Cycle: "0" in place of a "1" for the "X" flag bit for each word representing T_x.

F. SAMPLING SIGNALS

1. Data Sampling Pulses: X_a, Y_a, Z_a, X_t, Y_t and Z_t.

a. Sampling Time: 7th bit in word (count "6")

2. Sync Analog Sampling Pulse

   a. Sampling Time: First bit in every word (count "0").

3. "X" Flag Sampling Pulse

   a. Sampling Time: Count "5" if "X" flag = 1.

   b. Input Sampled: Sync analog dc voltage

Most of the features of the data format discussed above are observable in the FF16 waveform of Figure 5 which shows the output format for a typical readout cycle. The count "0" and count "6" read-in strobes shown in the central waveforms in Figure 5 indicate the relationship of the sampling times of the analog data relative to the digital output of FF16.

The top seven waveforms shown in Figure 5 represent both gated and direct outputs from a three-stage binary counter in Board A. A system clock operating at 12 kHz provides the input pulses. Four waveforms at 3 kHz and four at 1.5 kHz supply clock pulses of various phases to the A/D converter in Board C. The negative output interval in the waveform of FF17 illustrates the time interval during which the normal NRZ data format is replaced by the RZ format of the 5-bit synchronizing signal.

From the above discussion and from Figure 5, it can be observed that the transmitted data consists of 15 acceleration readings and one temperature reading every 0.32 seconds, thus giving a system frame rate of 3-1/8 frames per second. Data transmission is continuous and sampling of acceleration resumes without interruption upon completion of a temperature readout cycle. The operation of the system will be described in the following paragraphs starting from convenience at the beginning of an acceleration readout cycle.

At bit count "0" analog gate G32 in Board B (Figure 4) is sampled and the output is supplied to the A/D converter in Board C. The dc input to gate G32 represents the analog equivalent of the sync code (11101); therefore, the five bits generated by the A/D converter in the interval from count "0" to count "4" will become the sync code for the word. Provision for a "zero" for count "5," the flag bit, is accomplished by adjusting the sync analog voltage such that the output of the A/D converter at count "5" will normally be a zero.

Identification of words representing the output of the X axis accelerometer is accomplished by making use of an "X" flag identifying pulse which is generated in the logic circuitry during the time interval in which X-axis data is to be transmitted. The X-flag is used to obtain a second sample of the analog representation of the

sync code at count "5." Because the first digit of the sync code is a "1," the bit generated for the count "5" interval will be a "1" instead of the usual "0." The four remaining bits of the sync code are prevented from occuring by the readin of new data which proceeds as follows.

At count "6" (bit 7) one of gates 33 to 38 in Board B will cause one of the acceleration or temperature analog inputs to be sampled and read into the A/D converter. The actual input sampled depends on which of the six readin strobes, X_a, Y_a, Z_a, X_t, Y_t or Z_t is present. The design of the A/D converter is such that, as a consequence of each readin operation, the A/D converter is cleared of any residual data which may have been left from a previous conversion. Thus, after the commutated output of Board B has been transferred to Board C at count "6," the conversion to serial digital form proceeds automatically independent of sync or any other data previously present in the A/D converter. From count "6" until count "20" the A/D converter generates a 14-bit serial binary representation of the sampled signal, high order first. The last four bits of output are not necessarily meaningful since the design target for accuracy in the initial design was 0.1 percent. However, a 14-bit design is used in the present system both to provide added resolution and also to allow for future improvement in accuracy with minimum redesign effort.

The serial output of the A/D converter is applied to a 70-kHz subcarrier oscillator in Board D. The frequency of the 70-kHz oscillator is fully deviated to either 59.5 kHz or 80.5 kHz depending on whether the digital output represents a "one" or "zero." The subcarrier output is used to frequency modulate a 1680-MHz L-band transmitter module. The output of the transmitter is applied to a quadraloop antenna which is used to telemeter the data to the ground station.

DC power for the A/D electronics is supplied by a conventional short circuit-proof dc-to-dc converter module. The dc-to-dc converter is designed to accept dc input power of +7V to +10V at 1.5 A from the primary battery source and provide -17V, +17V and two isolated outputs, one at 5V and one at 28V. A regulator in the ac portion of the converter is used to achieve a 3-percent accuracy figure for all dc outputs of the converter. The +17V and the -17V outputs are further regulated in Board D to produce voltage outputs of +15V $\pm$0.5 percent and -15V $\pm$0.5 percent, respectively. A +2.5V $\pm$0.05 percent and a -2.5V $\pm$0.05 percent supply in Board D are used to supply precision dc reference voltages for the A/D converter.

SECTION IV

DETAILED CIRCUITRY

1. BOARD A, LOGIC CIRCUITS

Board A contains the circuitry used to generate the timing and control pulses required by the signal processing system. The schematic diagram for Board A is shown in Figure 6. The 12-kHz system clock is generated by a temperature compensated unijunction oscillator consisting of complementary unijunction transistor, Q1, and associated circuitry. Resistor R1 provides the compensation for temperature changes in Q1. The output of Q1 is amplified by Q2 and applied to a divide by 4 counter consisting of flip-flops FF1 and FF2. The output of FF2 and the outputs of Gates G1 and G2 supply clock pulses of the various phases required by the A/D converter circuitry at the system bit rate of 3 kHz.

Outputs at the word rate (1/20 of bit rate) are accomplished by using a divider composed of five flip-flops, FF3 through FF7. Flip-flop FF3 and FF4 are binary stages while flip-flops FF5, FF6 and FF7 are connected as a divide by 5 counter using the "J" and "K" input gates. Gate G3 is used tc initially set in a "1" in FF7 in order to insure the proper starting conditions. Gates G4, G5, G6, G8 and G9 accept inputs from the divide by 20 divider (1/2 x 1/2 x 1/5) and are used to generate sampling pulses for bit positions 1(count 0), 6(count 5) and 7(count 6) of each word. Strobe pulses for use in axis selection are generated by applying the output of FF7 to a divide by 3 counter consisting of FF8 and FF9. Gates G12, G13 and G14 accept outpus of FF8 and FF9 and also the count "6" output of G7; and, in turn generate strobe pulses X_a, Y_a and Z_a. The X_a pulse is used to sample the X axis accelerometer at bit 7 (count 6) of the X word. Similarly the Y axis is sampled by Y_a during the Y word which follows next and finally the Z axis is sampled by Z_a to complete an acceleration readout cycle. Acceleration readouts continue for 15 uninterrupted cycles. A divide by 16 counter consisting of FF10, through FF13 accepts inputs from FF9 and generates an output after the 15th readout cycle to reset FF14. The output of FF14 in turn disables Gates G12, G13 and G14 so as to inhibit acceleration strobes X_a, Y_a and Z_a during the next readout cycle. Instead, Gates G15, G16 and G17 are enabled to produce the temperature strobes X_t, Y_t and Z_t. These strobes are used to substitute three temperature samples in place of the usual three axis acceleration sample.

When one complete temperature readout cycle has been completed, the output of FF9 presets FF14 to begin the next sequence of 15 acceleration readouts.

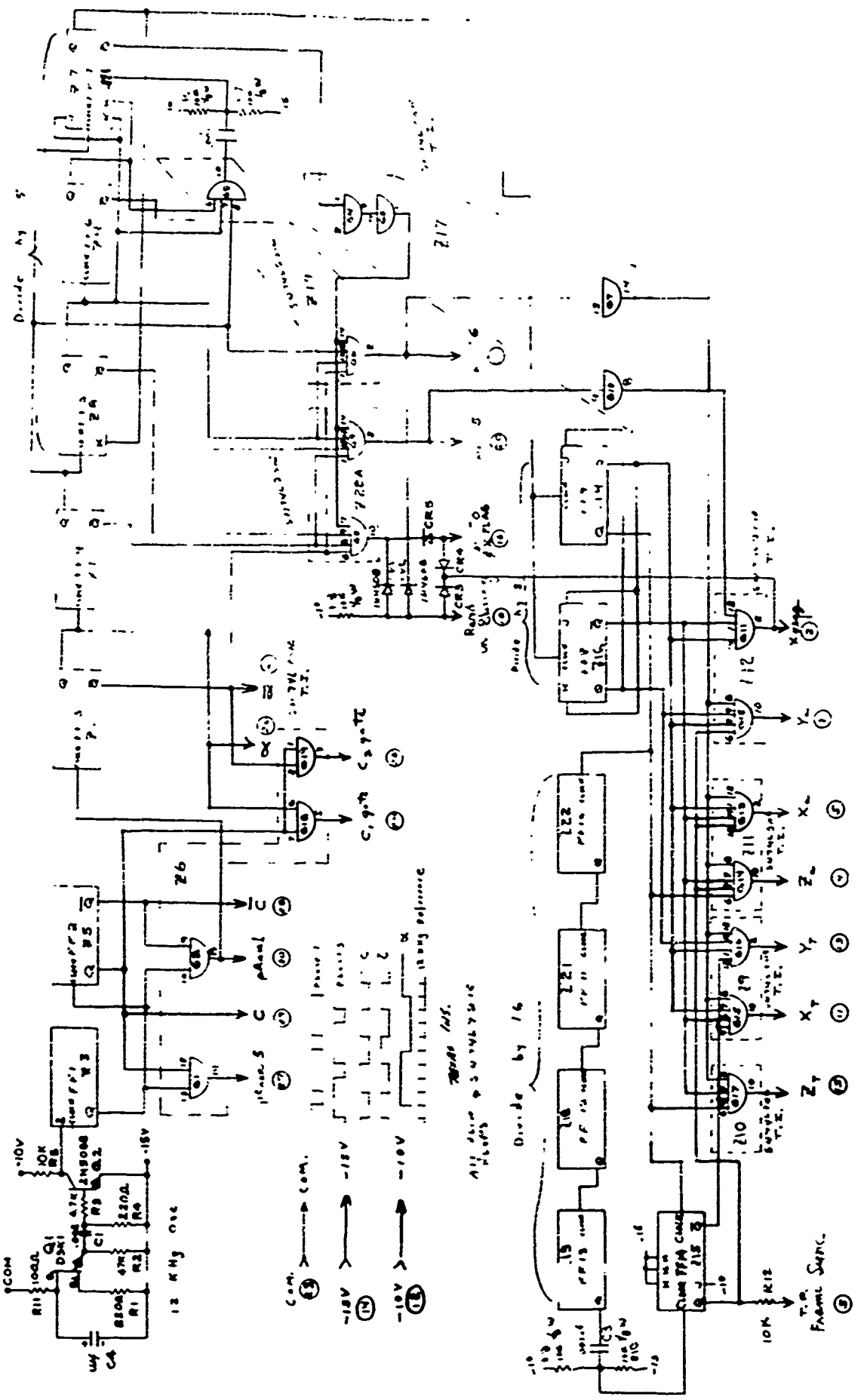


Figure 6. Logic diagram of Breadboard Schematic I.

2. BOARD B, COMMUTATING INPUT GATES

The set of input gates which are used to read in acceleration, temperature and analog synchronization data into the A/D converter of the processing system are shown in Figure 7. Gate G32 is used to read in the analog voltage representing the sync code. At count "0" (and again at count "5" if X flag = 1) the dc voltage at the arm of R2(2.07V nominal) is applied to the input of the A/D converter by means of field effect switch transistor Q1. This is accomplished by applying a negative (low) input to G32 which in turn causes the output of G32 to become more positive (high) than the input. Because of the emitter connections of driver transistors Q2 and Q3 to Gate G32 and because both bases are connected to a common resistor R8, the negative input to G32 will cause transistor Q2 to conduct and transistor Q3 to become cut off. This will reduce the bias across R6 to zero volts and cause Q1 to switch to the "on" state so as to couple the output of R2 to the A/D converter. At the end of the count "0" bit interval, the input to G32 will again become more positive relative to the output of G32, thereby causing Q2 to become cut off and Q3 to conduct. The output current of Q3 will flow through R6 producing sufficient bias to hold Q1 at the "off" state for the 19 remaining bit intervals of the word.

The action of read-in gates G33 through G38 at count "6," the time of data readin, is similar to the action described above for Gate G32 at count "0." In place of R6, however, a resistive divider circuit (R11 and R13 in the case of Q4) is used to bias the gate of the selected FET switch transistor Q4, Q7, etc., to the potential assumed by the input A/D converter without direct conductive contact. This arrangement avoids any loading effect on the selected accelerometer (temperature) sensor or on the input to the A/D converter. This is quite important because the output impedance of the accelerometers is moderately the high and the input impedance of the A/D converter is very high. The loading of the accelerometers and the A/D converter input could also have been avoided by the use of an insulated gate field effect transistor (Mosfet) in place of the junction FET used for Q1, Q4, etc. However, because of the large voltage swings required to switch from full off to full on, more switching noise (at least double in the case of the 2N3631 transistor) would have been introduced into the A/D converter circuitry had this type of device been employed.

3. BOARD C, A/D CONVERTER

The major purpose of the circuitry contained in Figure 8 is to obtain a digital representation in NRZ (non-return to zero) form of the analog input samples supplied by the commutating gates. As a secondary function, the circuitry in Board C also generated the system synchronizing code in RZ (return to zero) format.

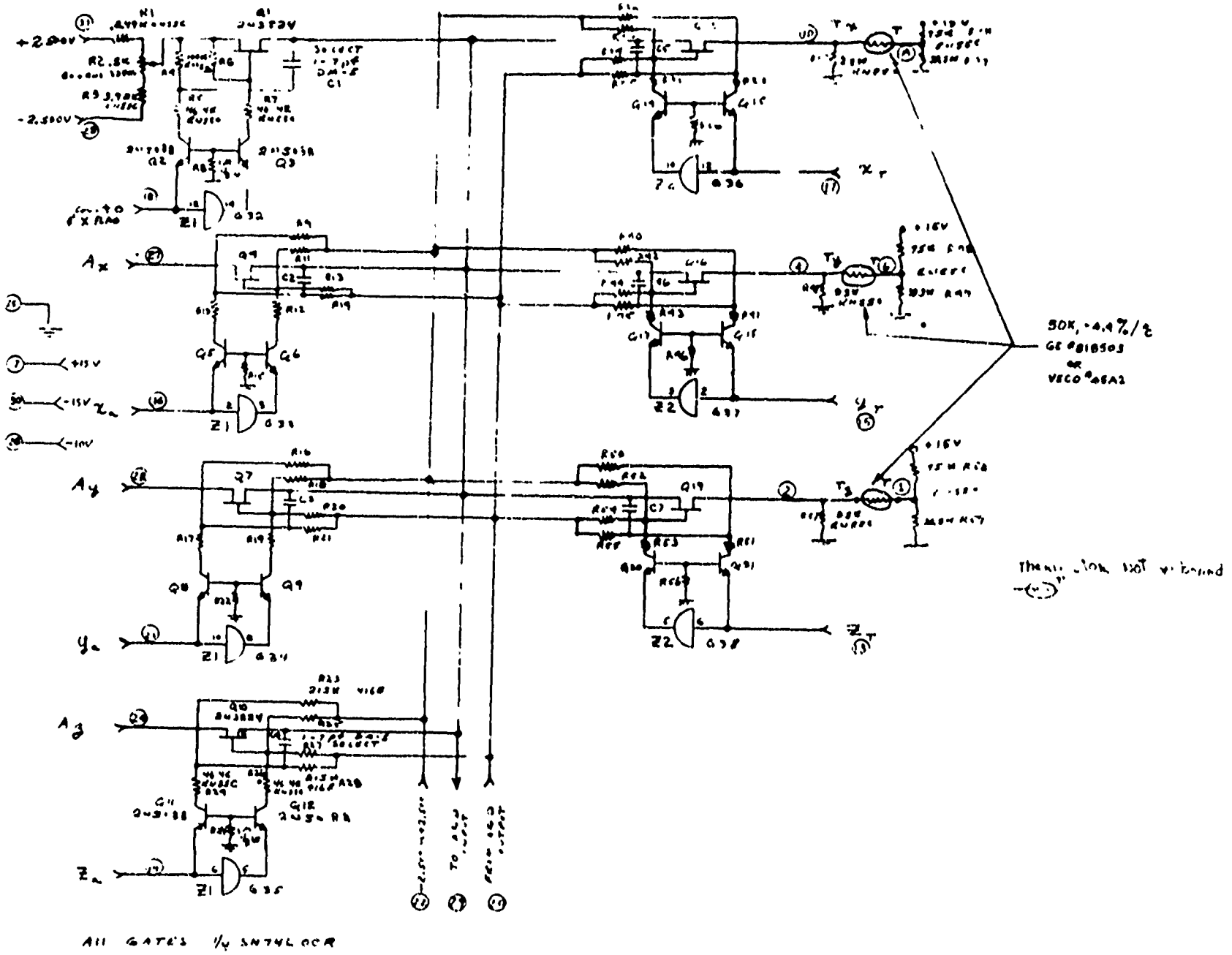


Figure 7. Schematic of commutating input gates.

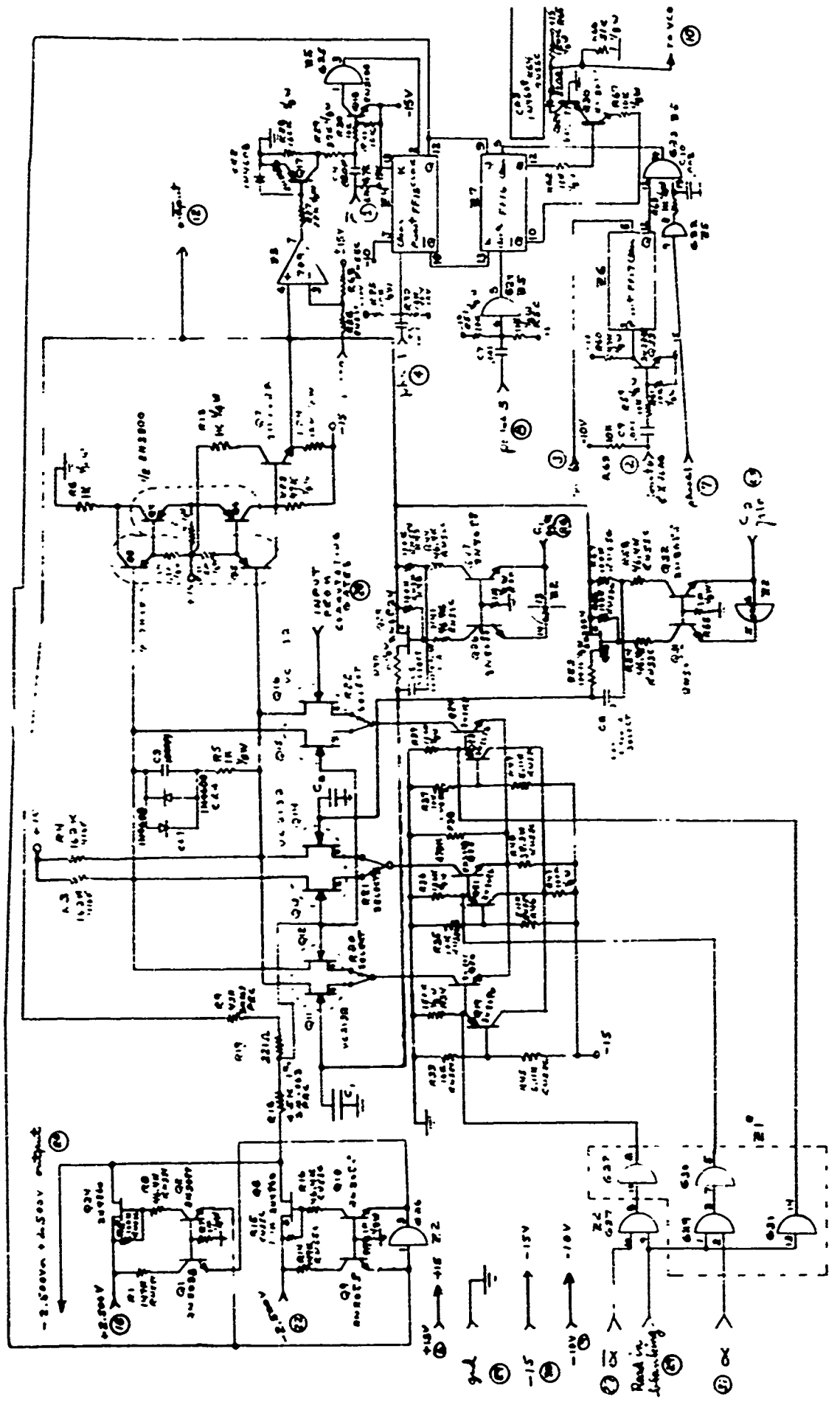


Figure 8. A to D Converter for Breadboard II.

a. A/D Converter Circuitry

A serial conversion technique is employed for the translation of data samples from analog to digital form. The primary advantage of this method is circuit simplicity and consequently realization of minimum size and weight for the overall system. The first step of operation of the serial conversion technique consists of reading in an analog sample and amplifying in a very precise "times two" amplifier. The doubled value is compared against a full scale reference voltage (5V) by a comparator module (Z3). If the result is greater than the reference voltage, an electronic switch (Q34) is used to subtract a voltage equal to the full scale reference voltage from the doubled value. The resulting difference is stored in analog form as residue #1 in capacitor C1 shown in Figure 8. If a subtraction has been made, a "one" is transmitted for the duration of the first bit interval to indicate that the voltage level of the analog input sample was at least 1/2 of full scale. If no subtraction has been performed, a "zero" is transmitted and the doubled value is stored in C1 as residue #1.

For the second bit interval the residue #1 voltage, stored in C1, is doubled and compared as before with the full scale reference voltage. A subtraction of the reference voltage is again made if the doubled value of the residue is greater than the full scale reference voltage. The result of the second comparison (and subtraction if required) is stored in capacitor C2 as residue #2. If a subtraction took place, a "one" is transmitted for the duration of the second bit interval to indicate that the voltage level of the analog input sample was at least 1/4 or 3/4 of full scale depending on whether the first bit was a zero or a one. Again, if no subtraction is made during the second bit interval a zero is transmitted for the second bit.

The above process is continued for 7 cycles (14 steps) with the even valued residues being stored in C2 and odd values being stored in C1. For the first 8 to 10 steps in the conversion process the error in the digital approximation will be reduced by a factor of two for each additional step. After the tenth step a point of diminishing returns is reached and second order effects such as noise generated by the dc-to-dc converter and the logic circuits place an assymptotic limit on system accuracy. However, if suitable care is exercised in the design and layout of the converter, an accuracy of ± 1 bit appears to be attainable at least on a short term basis, for up to a 14-bit system.

The method by which the circuit shown in Figure 8 performs the serial A/D conversion functions described above is as follows:

(1) Doubling of Input Sample. During read-in operation, transistor pair Q15 and Q16 are gated on and Q11, Q12, Q13 and Q14 are gated off. Transistors Q3, Q4, Q5, Q6, Q7 and the differential input pair,

Q15 and Q16 form an operational amplifier in which feedback resistors, R9 and R18 insure unity (1.000) gain inverting amplification for signals appearing at the outputs of Q34 and Q8. The same resistors establish a gain of 2.000 for inputs at Pin 28 of the circuit board. Inputs at Pin 28 will not be inverted.

(2) Doubling of the Residue in C1. This is similar to #1 except that Q15 and Q16 are gated off and Q11 and Q12 are used as the input pair for the operational amplifier. Amplification of the residue in C1 will be with no inversion.

(3) Doubling of the Residue in C2. Same as #2 except that Q13 and Q14 are gated on to be used for the input pair.

(4) Subtraction of the Reference Voltage. As a result of the bipolar nature of the accelerometer outputs, data inputs which normally have to be accepted by the A/D converter will be in the range of -2.500V to +2.500V. For this reason the A/D converter is designed with a built-in bias of -2.500V for system zero. Thus a 0V signal is converted as if it is at +2.500V and +2.5V signal is converted as if it is at +5.00V. Also, the +2.500V reference behaves as the 5V full scale reference voltage referred to in the general description of the principle of operation.

If a subtraction is to be made (as indicated by the presence of an output pulse from comparator Z3 and a consequent change of state of FF15 to the "1" state) the output of FF15 will cause Q2 to turn on switch Q34 and Q10 to turn off switch Q8. As a result of this action, the normal -2.500V output of Q8 at the input of resistor R18 will be switched off and the output of Q34 will change this input to +2.500V. Because this voltage is applied to the unity gain inverting input of the operational amplifier, the +5V increase in voltage at the input to R18 will be converted to a 5V decrease (subtraction) in voltage at the output of the operational amplifier (emitter of Q7).

(5) Storage of Analog Residue in C1. Normally C1 is in the storage (hold) mode. Leakage of charge from C1 during a bit interval is negligible as a result of the high input impedance of FET transistor Q11 and the low $I_{d\ off}$ rating of Q25 (less than 10^{-10} A). Read in of the updated analog residue is initiated when a negative pulse, C_1 is applied to Pin 26 of the A/D converter board causing Q26 to turn off. This in turn causes the gate-to-source voltage of Q25 to go to zero volts, turning Q25 full "on," thereby connecting the output of Q7 to capacitor C1 for the duration of the pulse C_1. At the end of the C1 pulse the voltage across capacitor C1 will have charged to the same potential as the output of the operational amplifier. When the C_1 pulse terminates, the voltage across the storage capacitor will remain at the value it was at just before the termination.

(6) Storage of Analog Residue in C2. Similar to #5 except that pulse C_2 is used in place of C1 and switch transistor Q28 is used in place of Q25.

(7) Gating of Differential Input Stages of the Operational Amplifier, Q11, Q12, etc. (This will be explained for only stage Q11 and Q12 because the operation of Q13-Q14 and Q15-Q16 is similar). Transistor stages Q11 and Q12 are turned on and off by means of a gated constant current source in the source circuit. For "on" operation transistors Q19 and Q20 are biased on by resistor network, R33 and R45. The current through Q20 is a constant and is determined by emitter resistor R48. The collector current of Q20 is in turn applied to the sources of Q11 and Q12 to turn these transistors on. If Q11 and Q12 are to be turned off, the logic level of either the read-in blanking signal or clock pulse $\bar{a}$ will be at a low state (negative) which causes the output of G27 to be high. Gate 28 inverts the output of Q27 thereby causing the base of Q20 also to be low. This action cuts off Q20 and thus reduces the constant current source to zero thereby causing Q11 and Q12 to become cut off. Under normal operation at least one of the three differential input pairs of the operational amplifier is conducting. Resistor R48 supplies the current for the pair of input transistors which are gated on. Gate G30 is used to turn on Q13-Q14 and gate G31 is used to turn on Q15-Q16.

b. Sync Code and Output Formatting Circuits

As described earlier the sync code is generated by performing a 6-bit A/D conversion on a fixed voltage. The fixed voltage is nominally 2.07 volts and represents the analog equivalent of a digital output of 11101010. However, the conversion is allowed to proceed only for the first six bits of a word, the remaining 14 bits being reserved for data.

The serial digital output of the A/D converter is available in return to zero format with "one" bits having a duty cycle of 75 percent. In order to convert this format to NRZ for the data and RZ for the sync pulses, the output of the compare flip-flop FF15 is transferred to flip-flop FF16 by the Phase 3, 3 KHz clock pulses. For NRZ transmissions each bit of the data remains in FF16 until the read-in of the next bit 333 μsec later. In the case of the sync bits which occur during the first five bits of a word, five 3-kHz clock pulses at Phase 1 time are gated into the clear input of FF16 to generate the RZ format. The gating action required to produce the five clear pulses is started by the trailing edge of the count zero output pulse which sets FF17. The output of FF17 opens G23 and allows Phase 1 pulses to pass through. At the end of six pulses of Phase 1, flip-flop FF17 is reset by a pulse of Count 6 time. This turns off G23 and prevents the application of clear pulses to FF16 for the remaining 14 bits of the word.

When FF17 is reset at Count 6 time, the trailing edge of the X Flag pulse appears in differentiated form at the preset input of FF17. Thus both the Q and the $\bar{Q}$ outputs of FF17 will be at a high state for a short interval of time ($\approx$ 30 μsec). During this short interval of time, one additional Phase 1 pulse of narrower duration from the first five will reset FF16 to establish an RZ format for the flag bit. If an NRZ format is desired for the flag bit, this can be accomplished by deleting the X Flag strobe pulse portion of the input signal at pin 2.

The output of flip-flop FF16 contains the complete digital message suitably formatted for transmission. Because an FM-FM system is employed for modulation the output of FF16 is applied to a subcarrier oscillator in Board D. A pair of NPN buffer transistors Q29 and Q30 are used to translate the -10 to -15V output level of FF16 to the 0 to +5V level required by the subcarrier oscillator.

4. BOARD D, REGULATORS AND VCO

The regulator portion of the circuitry contained in Board D is shown in schematic form in Figure 9. The regulator accepts +17V and -17V dc power from the dc-to-dc converter and generates +15V $\pm$ 0.5 percent, -15V $\pm$ 0.5 percent, +2.500V $\pm$ 0.05 percent and -2.500V $\pm$ 0.05 percent. The regulator for the +15V output consists of a zener reference diode, D1, differential stage, Q2 and Q6, and an output section consisting of Q5 and Q7. During normal operation a sample of the +15V output is delivered to the base of Q6 by means of resistors R5 and R6. The base voltage of Q6 is compared to the reference voltage provided by D1 at the base of Q2. If a voltage error is present, it is amplified by Q5 and Q7. This causes the +15V output to change by an amount and in the direction required to cause the error to approach zero. The degree to which the error approaches zero is dependent on the gains of Q2, Q6, Q5 and Q7.

The initial "turn on" of the supply is insured by a low pinch-off field effect transistor, Q1. When full output is reached, Q1 becomes biased to cutoff and thus does not interfere with regulation operation.

Resistor R2 and transistors Q3 and Q4 supply the collector of Q2 with a constant current high impedance load so as to maintain a high gain for stage Q2. Diodes D2 and D3 place a limit on the maximum drive level available at the base of Q5, thereby providing short term protection for the regulator in the event that the +15V output is accidentally short circuited.

The operation of the -15V regulator is similar to that for the +15V regulator. The same circuit is used but is in complementary form, i.e. NPN transistors used in place of PNP's and vice versa.

The +2.500V supply is derived from the 6.4V precision voltage developed by reference diode D7. Resistor R21 is used to obtain a 2.500V sample of this voltage and supply it to a unity gain non-inverting type 709 operational amplifier, Z2. The +2.500V output of Z2 is amplified and inverted in a second operational amplifier circuit Z1. Equal values are used for the feedback resistors (R25 and R26) associated with Z1; therefore, the output of Z1 will be at -2.500V.

The VCO portion of the circuitry in Board D is illustrated in Figure 10. The VCO consists of a temperature compensated voltage controlled square wave multivibrator circuit consisting of Q18, Q19 and associated

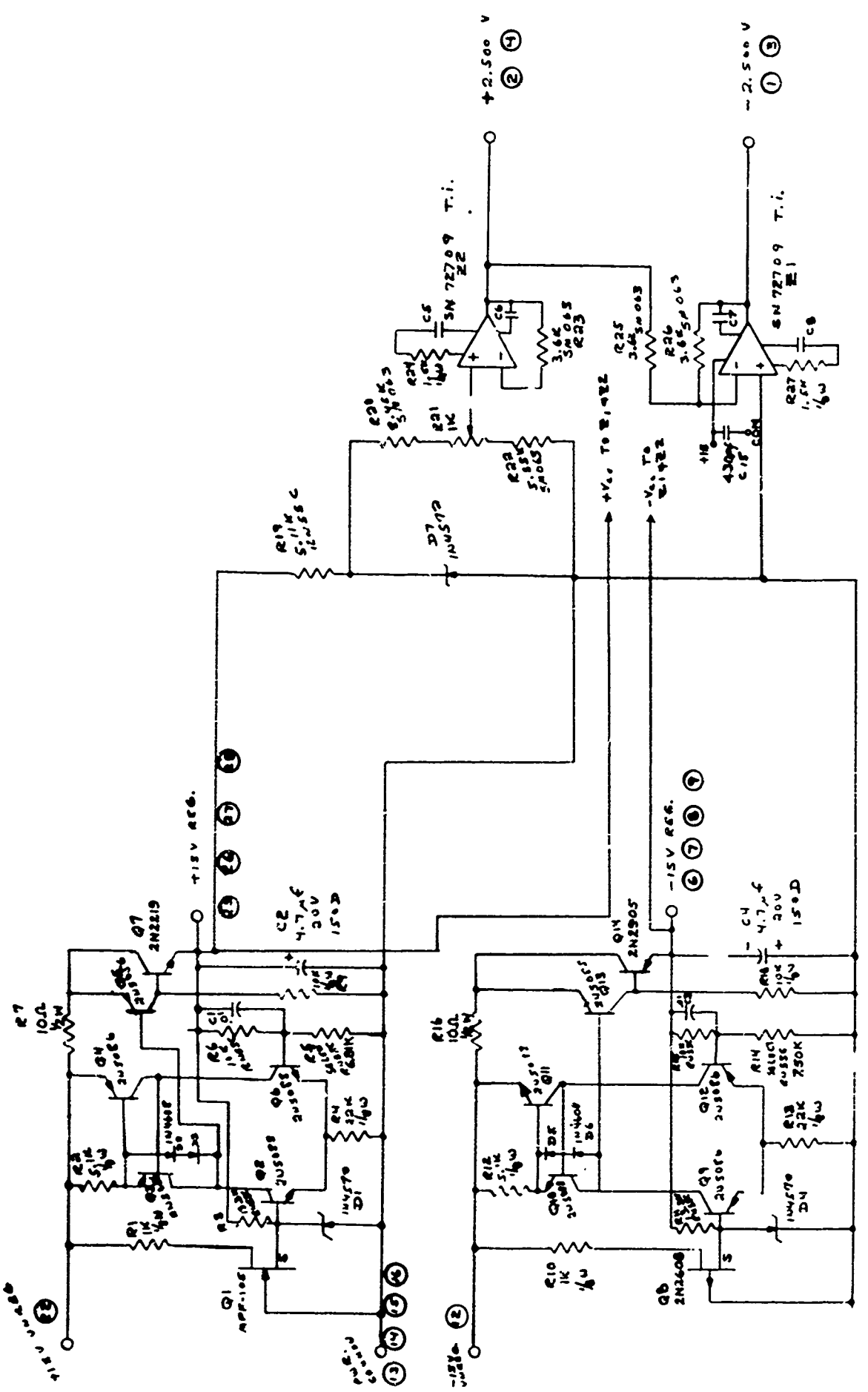


Figure 9. Regulators & volt. ref.

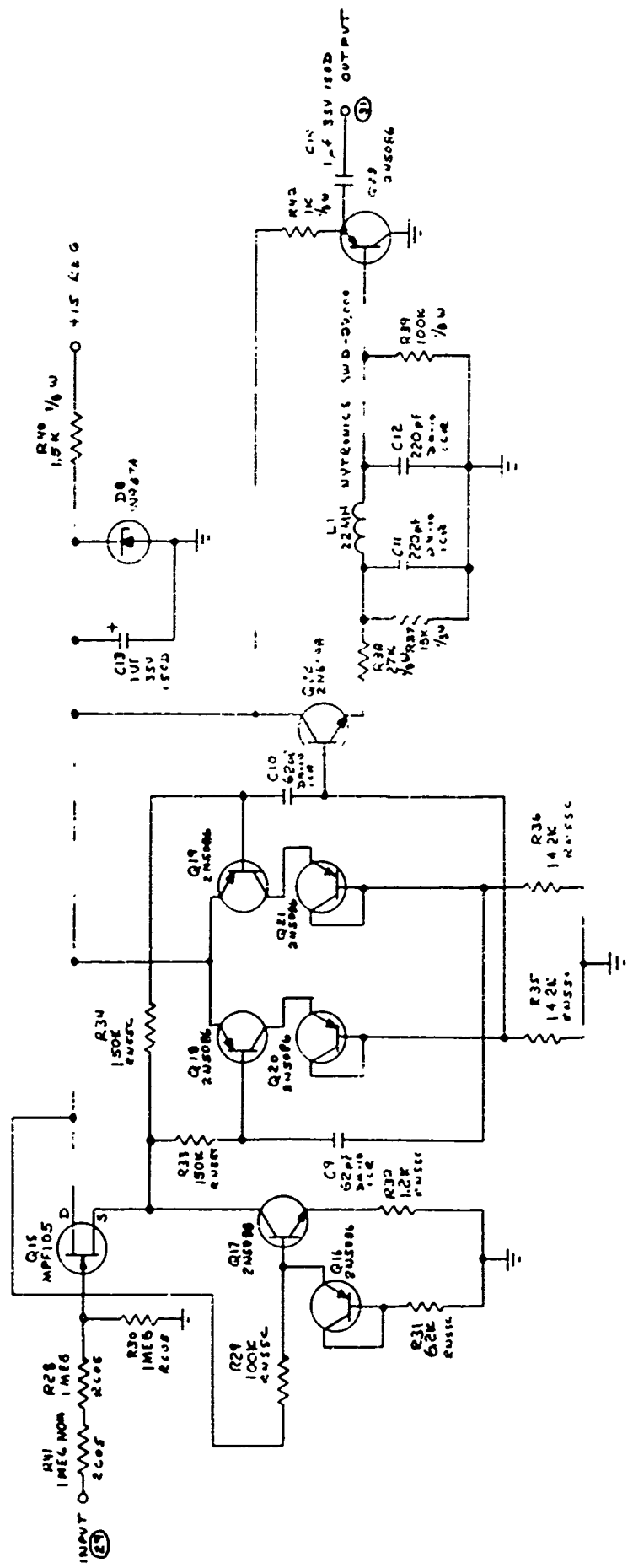


Figure 10. Schematic, 70K, VCO.

components. A field effect buffer stage Q15 provides a high impedance for input signals. Stabilization of operating frequency against changes caused by temperature variations is provided by diode connected transistors Q20 and Q21 which compensate for temperature induced changes in the base-emitter input characteristics of Q18 and Q19.

The squarewave output at the collector of Q20 is applied to a low pass filter via emitter follower Q22. As a result of the filtering action of C11, L1 and C12, the signal applied to the base of the emitter follower Q23 is essentially sinusoidal in shape. The subcarrier output of the VCO is used to modulate the 1680-MHz transmitter in the manner described previously.

5. DC-TO-DC CONVERTER

The dc-to-dc converter circuitry is shown in schematic form in Figure 11. The operating frequency of the converter is determined by a temperature compensated unijunction oscillator Q7. The output of Q7 is amplified by Q6 and applied to a flip-flop divider which produces a symmetrical squarewave output voltage. The outputs of the divider together with transistor stages Q1 and Q16 cause the current through R1 to commutate between common base transistor stages Q2 and Q15 so as to generate the required push-pull drive for the output stages. The output of Q2 is amplified by Q4 and Q5 while the output of Q15 is amplied by Q9 and Q8. The outputs of transistors Q5 and Q8 are applied in push-pull to output transformer T1. Regulation is provided by utilizing diodes CR9 and CR11 to sample a portion of the ac output voltage across the primary of T1 and compare the sampled waveform to a 5V dc reference provided by CR12. The output of CR9 and CR11 is used to divert the current supplied by R1 away from Q2 and Q15. This in turn tends to reduce the drive to T1 by reducing the drive to Q5 and Q8. Conversely, if the output signal across T1 tends to drop, CR9 and CR11 will conduct less and thus allow more current to pass through Q2 and Q15. This will increase the drive to Q5 and Q8 thereby tending to increase the drive to T1.

If an overload condition or a short circuit condition in the load occurs, the voltage across R13, the current monitoring resistor, increases and turns off Q11. The output of Q11 is amplified by Q12 and applied to Q3 and Q10. Transistors Q3 and Q10 are used shunt out the input drive to Q4 and Q9 and thereby to limit the drive to Q5 and Q8 to a safe value. The value of short circuit (or overload current) is determined by the value of the current monitoring resistor R13 and the reference voltage drop across R21.

Conventional rectifier circuits associated with the transformer output windings are used to provide outputs of +17V at 65 mA, -17V at 62 mA, an isolated 5V output at 32 mA, and an isolated 28V output at 150 mA.

Protection against reversal of external input power polarity or of battery charging polarity is provided by the external diodes (IN4060 and IN4608) shown in system diagram in Figure 4.

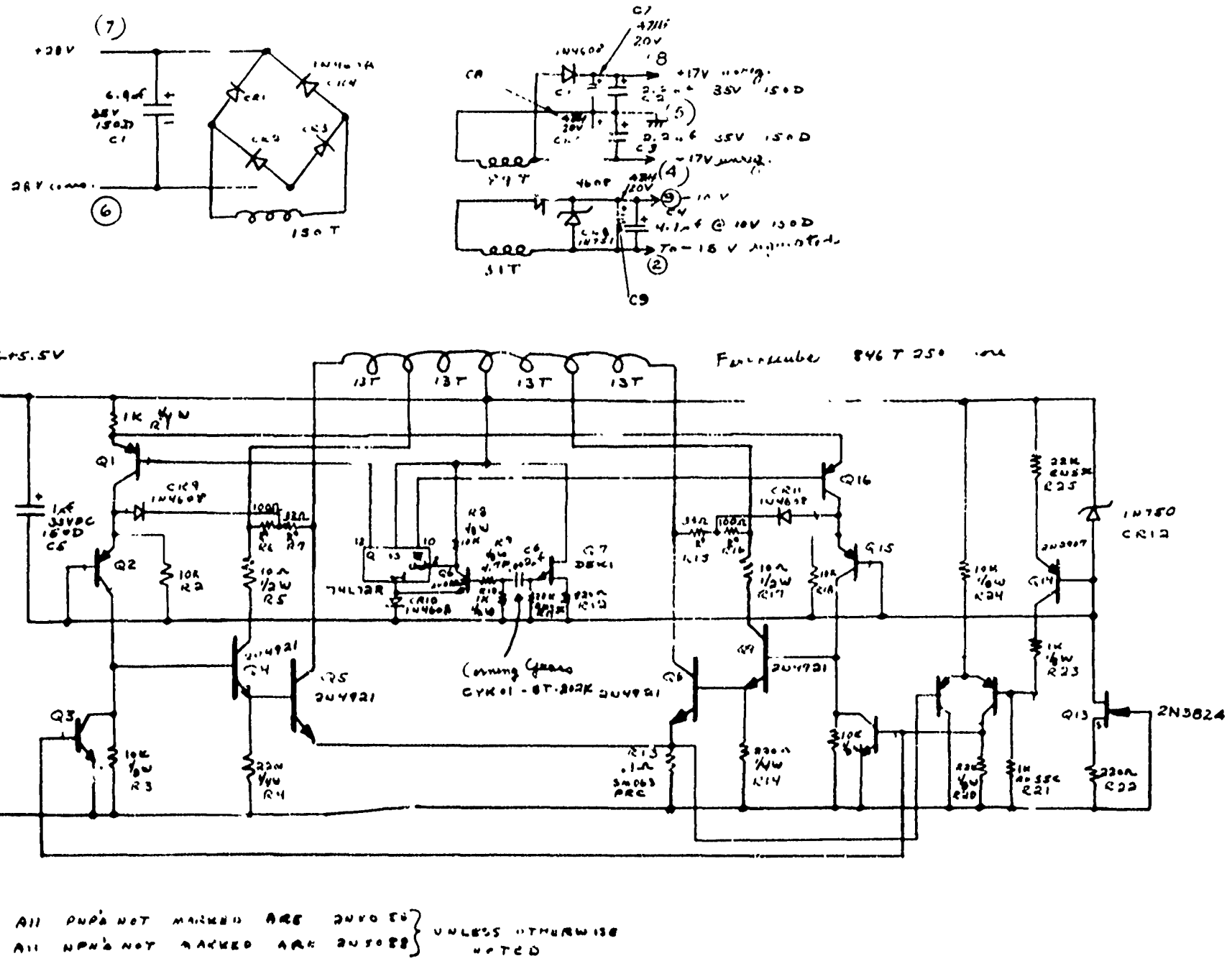


Figure 11. Power supply.

SECTION V

MECHANICAL DESIGN

1. NOSE CONE

Several modifications were made to the mechanical design of the nose cone and release mechanism which was developed under previous contract AF19(628)-5122. The changes consisted of redesign of the nose cone to utilize aluminum rather than magnesium, redesign of the split clamp ring to improve bending rigidity and redesign of the release mechanism. A simple explosive bolt release mechanism was designed and sucessfully replaced the more complicated slide-bar release mechanism. Fragmentation of the bolt is contained within the payload adapter and therefore cannot affect the sphere.

The magnesium split nose cone was developed under previous contract AF19(628)-5122. Although this material is adequate for this application on a small scale, it is not suitable with respect to wide-scale operational meteorological use of the inflatable sphere system. Its primary drawback is high cost; secondarily, the material has inherent corrosion problems and potential machining fire hazards. Two other materials, fiberglass and aluminum, were considered as reasonable substitutes. Fiberglass appeared to be most suitable with respect to satisfying the low-cost production requirements. It was envisioned that the nose cone halves could be molded exactly to the required dimensions thus obviating machining costs. However, investigation proved that this would entail considerable development cost in order to obtain the dimensional accuracy and uniformity required. Aluminum was then selected as the compromise material. It is lower in cost and more readily available (as a casting) than magnesium. Also an increase in weight of the nose cone was allowable since the original magnesium design was only 12.5 pounds and the maximum allowable payload weight was 14 pounds.

The vendor who was selected to manufacture the castings did not produce a pattern which accurately reproduced the desired cast shape. The castings which were produced are oversized about 1/8 on the diameter. However, they are useable if properly machined with a taper at the adapter end as shown in Figure 12. There is some advantage to the oversize nose cones in that additional internal volume is available for packaging the sphere.

Another feature of the aluminum nose cone is the modified attachment of the rubber sheet which cradles the sphere package when assembled. The new attachment stretches the rubber across a chord of the clam-shell nose cone hemisphere rather than across the diameter. Thus, the pinching effect of the mylar sphere material is reduced when assembling the system.

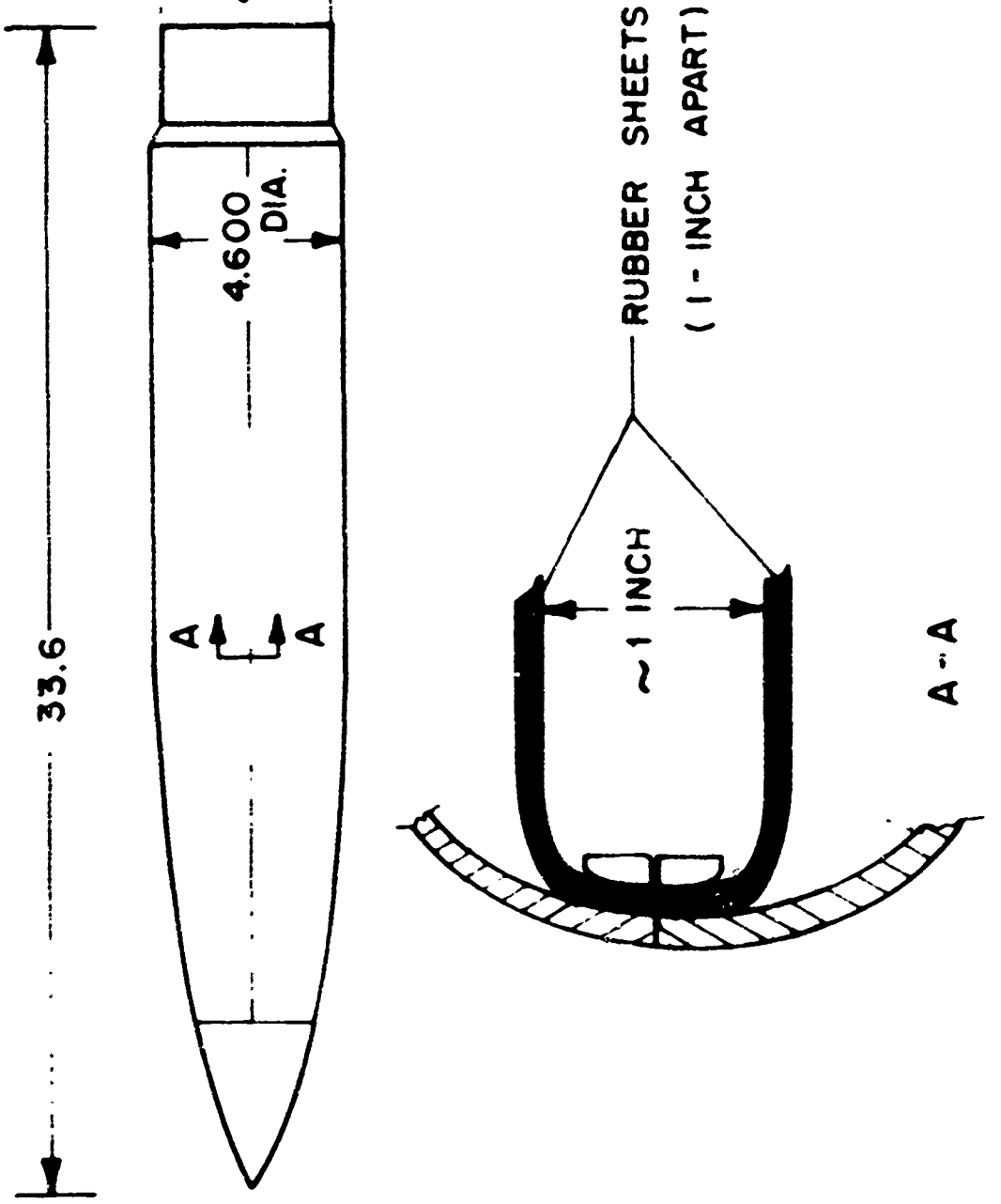

01ED71-105
4.445 DIA.
ARCAS MOTOR
4.600 DIA.
33.6
A
A
RUBBER SHEETS
(1-INCH APART)
~1 INCH
A-A

Figure 12.

2. RELEASE MECHANISM

A simple release mechanism for the inflatable sphere split nose cone was designed, fabricated, and tested. The device consists of two aluminum blocks which are held together with a size 10 explosive bolt. Figure 13 shows the concept schematically. When the bolt, D, fires, part A is ejected and parts C are released thereby releasing the two halves of the split nose cone. The same firing circuit is used for this release as was used for the original release mechanism designed under the previous contract AF19(628)-5122. Note the simplicity of manufacture of this device lends itself to production in the event the system is adopted for operational use.

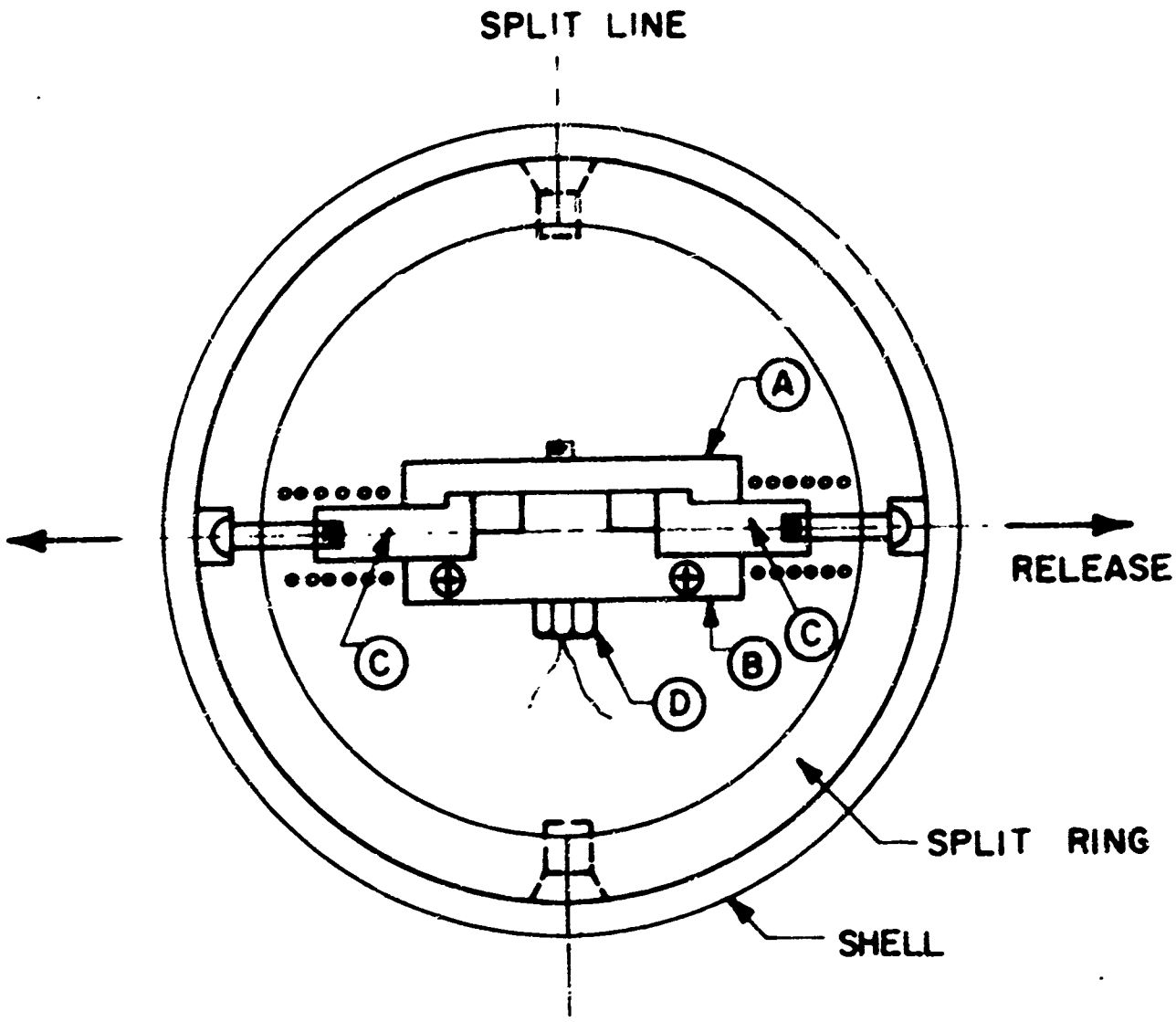


Figure 13.

SECTION VI

ERROR ANALYSIS AND TEST RESULTS

1. ERROR SOURCES

The three major sources of error in the falling sphere method of measuring density are: (1) mechanical (centrifugal acceleration effects, accelerometer misalignments, and vibration noise), (2) electronic (accelerometer errors, sampling errors, and A/D conversion errors), and (3) aerodynamic (inaccuracies in the determination of drag coefficient and errors caused by the distortions of the "semirigid" mylar sphere as a result of the drag forces encountered). With the exception of a discussion of accelerometer misalignment errors, only electronic sources of error will be discussed below because it is assumed that a sufficiently detailed consideration has already been given to mechanical and aerodynamic errors during the initial developmental program for the falling sphere experiment.

a. Accelerometer Mechanical Errors

The accelerometer package deserves comment because the Systron Donner model 5602-1A three-axis accelerometer which was used in previous falling sphere payloads has been replaced by three single axis Model 4311 accelerometers. The replacement accelerometers are located in a redesigned housing provided by GCA Corporation. The Model 4311 accelerometer is normally furnished with an alignment accuracy to the true sensitive axis of $\pm 1.0^{\circ}$. However, options specifying tighter tolerances down to about $\pm 0.1^{\circ}$ are also available. (See attached specification sheet for the 4311 accelerometer, Figures 14 and 15.)

By exercising reasonable care during the fabrication process, the alignment of the acceleration housing has been held to a tolerance of $\pm$ 0.2 degree. In order to obtain the best cost-performance compromise, the accelerometers were purchased to an alignment specification of $\pm$ 0.5 degree. However, acceptance test measurements on the 4311 accelerometers, which were received from Systron Donner, indicated a much lower error figure. Therefore, a maximum of $\pm$ 0.5 degree is a reasonable value to use for the overall alignment error for each axis rather than the anticipated $\pm$0.7 degree. This compares with an overall misalignment error of $\pm$ 0.5 degrees for the Model 5602-1A accelerometer.

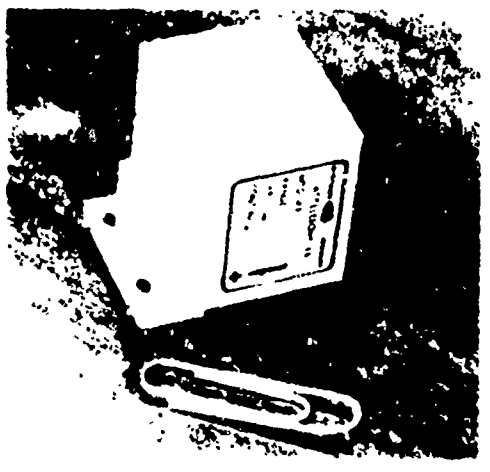
The individual misalignments of the sensitive axes of the three accelerometers may or may not contribute to an error in the determination of the magnitude of the acceleration vector. More specifically, misalignment errors of the three accelerometers are permitted to the extent that the three sensitive axes remain at right angles to each other.

Figure 14

HIGH PERFORMANCE MODEL 4311 SERVO ACCELEROMETER

INTRODUCING THE MINIATURIZED VERSION OF THE WELL-KNOWN DONNER MODEL 4310

Donner's new miniature version of its well-known Model 4310 is now in production. This accelerometer incorporates all of the widely accepted and qualified features of the Model 4310 and at the same time offers many more advantages not found in the Model 4310.



These features . . .

1. Smaller size (one-half the size of the Model 4310).
2. Same mounting and connector location standard.
3. Increased performance. . . A. Under temperature
   B. Under vibration
4. Design specified and performance rated for low cost platform use.
5. Unitized construction – no separate electronic packages required.

APPLICATION:

CHEYENNE HELICOPTER

THOR DELTA

AY Aircraft

A7 Aircraft

Specifications

ACCURACY

Null [illegible] B.F.S.L.	± 0.015% of F.R.
Hysteresis	0.01 of F.R.
Resolution	0.001 of F.R.
Null Repeatability	0.01 of F.R.
Zero Output vs. Null	0.05 of F.R.
Temperature Coefficient of Null	0.001% of F.R. F from 40 to 160 F
Temperature Coefficient of Scale Factor	0.005% of F.R. F from -10 to 160 F
Scale Factor Non-Linearity	0.05% of F.R.
[illegible]	0.002 g g at F.S.L. on SA
Temperature Coefficient of Scale Factor	0.005% F
[illegible] Repeatability	1.0 10 g g
Natural Frequency (Open Loop) Short [illegible] F. [illegible]	E.D. 150 to 250 Hz
Damping Ratio (Open Loop) [illegible]	E.D. 0.4 to 0.7 0.1

* Other ranges are available

** Also available [illegible] Axis Sensitivity, 1 0.02 g g
[illegible] 0.01 g g
[illegible] 0.005 g g

ENVIRONMENTAL

Temperature Range	Storage: -65 F to 200 F Operating: -40 F to +200 F
Shock Survival	100 g, 11 ms
Vibration Survival	15g RMS, 20-2000 Hz
Humidity, Salt Spray, Fungus, Sand, Dust	Hermetically Sealed (Meets MIL-E-5272C)
Ambient Pressure	0 to 5 Atmospheres Absolute

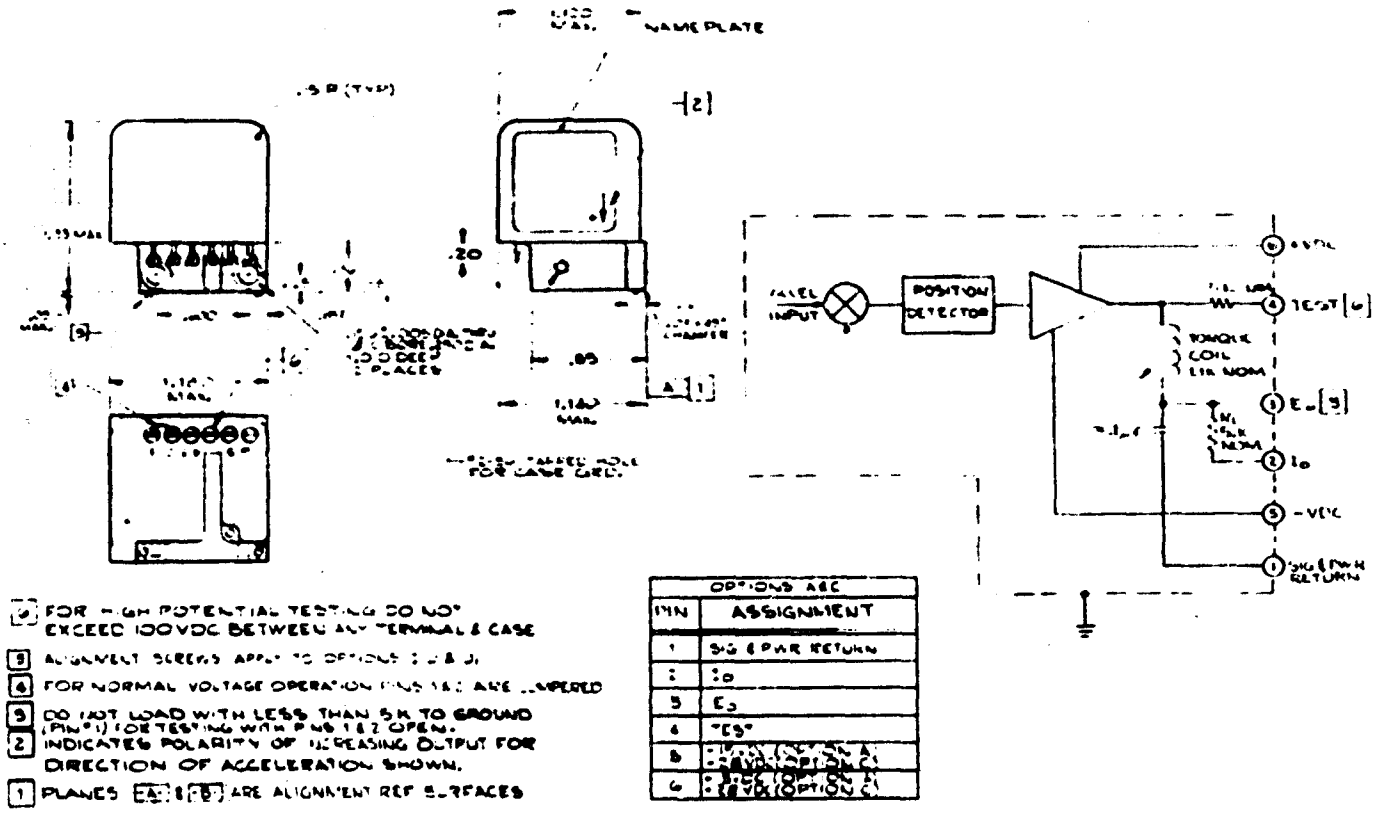
PHYSICAL

Range *	0.5 g to ±50 g
Voltage Output (Nominal)	±5 VDC (R_L = 5 K Ω) or ±15 VDC (R_L 5 K Ω) Telemetry: ±0.2 to ±4.8 VDC
Input Power	±15 VDC ± 10%, at ± 10 ma – or ±28 VDC ± 10%, at ± 15 ma Telemetry: ±28 VDC ± 10%, at 20 ma
Electrical Connector	Solder Terms
Case Alignment **	± 1 to True Sensitive Axis (½ to 2 m radians optional)
Weight	2 oz.
Physical Configuration	Rect. Case: E.D. Round Case: E.D.

SYSTRON DONNER CORPORATION

[illegible] 9455, U.S.A. • Tel: (415) 682-6161 TWX: 910 481 9429, Cable: SYSTRONDONNER

Figure 15



OPTIONS A&C	
PIN	ASSIGNMENT
1	SIG & PWR RETURN
2	I_o
3	E_o
4	"ES"
5	-15 VDC (OPTION A) -28 VDC (OPTION C)
6	+15 VDC (OPTION A) +28 VDC (OPTION C)

[2] FOR HIGH POTENTIAL TESTING DO NOT EXCEED 100VDC BETWEEN ANY TERMINAL & CASE

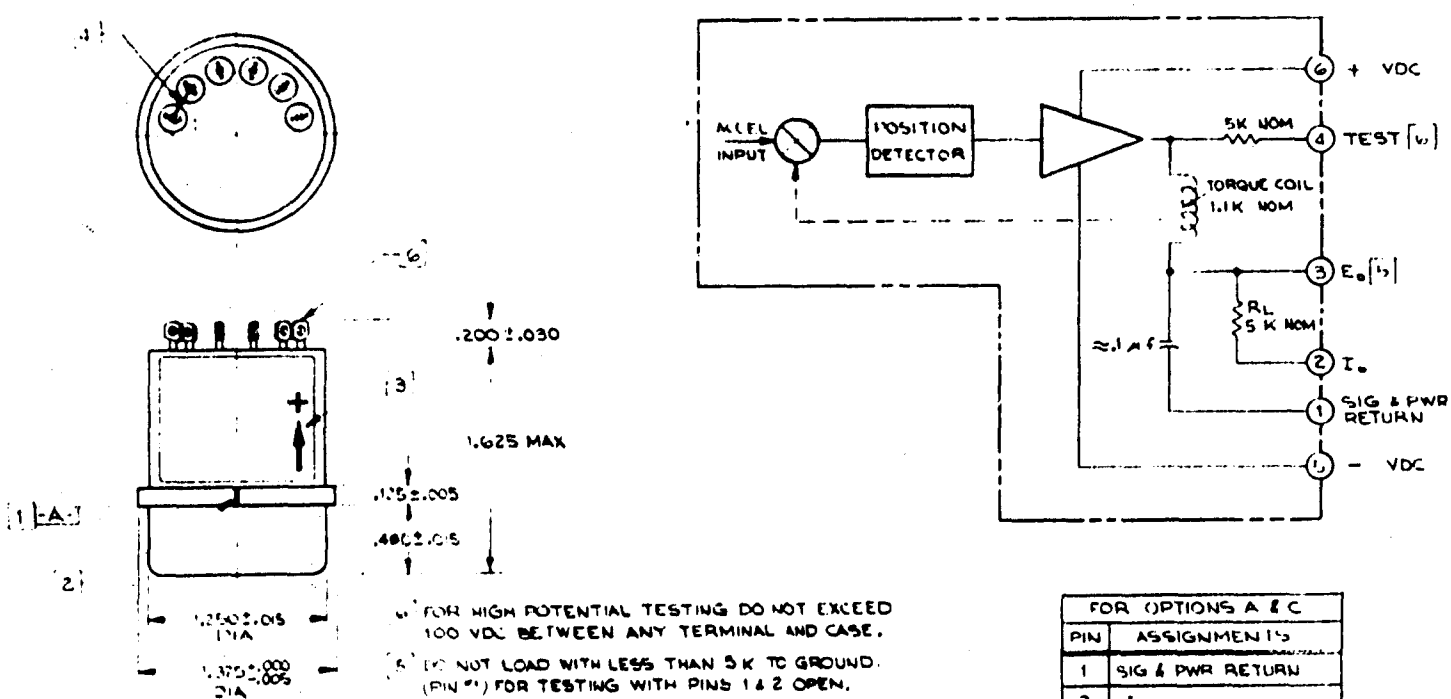
[3] ALIGNMENT SCREWS APPLY TO OPTIONS A, C & D.

[4] FOR NORMAL VOLTAGE OPERATION PINS 1 & 2 ARE JUMPERED

[5] DO NOT LOAD WITH LESS THAN 5K TO GROUND (PIN #1) FOR TESTING WITH PINS 1 & 2 OPEN.

[2] INDICATES POLARITY OF INCREASING OUTPUT FOR DIRECTION OF ACCELERATION SHOWN.

[1] PLANES [A] & [B] ARE ALIGNMENT REF SURFACES



FOR OPTIONS A & C	
PIN	ASSIGNMENTS
1	SIG & PWR RETURN
2	I_o
3	E_o
4	TEST
5	-15VDC (OPTION A) -28 VDC (OPTION C)
6	+15 VDC (OPTION A) +28 VDC (OPTION C)

[6] FOR HIGH POTENTIAL TESTING DO NOT EXCEED 100 VDC BETWEEN ANY TERMINAL AND CASE.

[5] DO NOT LOAD WITH LESS THAN 5 K TO GROUND. (PIN #1) FOR TESTING WITH PINS 1 & 2 OPEN.

[4] FOR NORMAL VOLTAGE OPERATION JUMPER PINS 1 & 2.

[3] ARROW INDICATES POLARITY OF OUTPUT FOR DIRECTION OF ACCELERATION.

[2] SCRIBE LINE INDICATES PIVOT AXIS WITHIN ±5°.

[1] PLANE [A] IS ALIGNMENT REFERENCE SURFACE.

This is so because a calculation of the direction of the acceleration vector is not of interest. The three accelerometer outputs are used only to determine the magnitude of the acceleration vector at each point of the flight. The values of acceleration magnitude are required for use in the drag equation to determine density. Acceleration magnitude is computed during the data reduction process after the flight using the relation $a_t = a_x^2 + a_y^2 + a_z^2$ where a_x, a_y, and a_z are the values of the accelerometer outputs corrected for offset errors and centrifugal force effects in the manner described below.

If the magnitude of the misalignment error of the sensitive axis of each of the accelerometers is at the same worst case value of θ_{max} degrees and if the directions of the misalignment are such as to produce a maximum error in the determination of acceleration magnitude, the value of this maximum error in terms of a percentage figure is given by

$$\% a_e = \frac{100 \Delta a_t}{a_t} \quad \frac{100 \sqrt{2}\, \theta_{max}}{180} \approx 2.5\, \theta_{max} \%$$

The payload aspect angle at which this maximum value of error occurs will depend on direction and magnitude of the alignment error for each accelerometer. However, the present degree of sophistication of the falling sphere experiment is such that the effects of payload aspect angle can be disregarded. For a θ_{max} value of 0.5 degree, the peak percentage error in acceleration determination will be $a_{e\,max} = 2.5 \times 0.5 = 1.25$ percent. This amount of error is considered tolerable in view of the fact that a reasonable estimate for the error in the determination of drag coefficient at these altitudes can be several times greater than this value.

b. Electrical Errors

The major categories of electronic errors are accelerometer errors and errors generated in the A/D converter. The error tolerances for the accelerometer are shown in the manufacturers specification sheets which are reproduced in Figures 14 and 15. The data sheets indicate that the zero output error could be up to $\pm$ 0.05 percent plus an additional $\pm$ 0.05 percent change for temperature variations of $\pm$ 30°C (0 to +60°C). Also, a scale factor change of up to $\pm$ 0.25 percent over the temperature range is possible.

c. In Flight Calibration

A convenient method of correcting for electrical offset errors which may be present in the accelerometers and in the A/D electronics is available as a consequence of the "zero" g reference point which exists when the rocket probe is at the apogee portion of its trajectory. During this time, a near vacuum condition prevails so that aerodynamic forces can be ignored. Thus, the only remaining force of interest

acting on the accelerometers is mechanical and consists of the centrifugal force resulting from the angular momentum of the sphere. Because of the nature of the accelerometer design, centrifugal accelerations are indistinguishable from the linear accelerations which are to be measured and thus appear as electrical offsets. Besides the initial zero output error and the offsets resulting from centrifugal forces, each accelerometer may have an offset attributable to a permanent zero shift resulting from stress during launch. Because the measurement portion of the falling sphere flight is of such short duration, the above accelerometer errors plus any offset errors which may be present in the electronics circuitry at this time will be constant during the measurement portion of the flight which immediately follows. Consequently, these errors can conveniently be subtracted from the raw data during the data reduction process.

2. ERRORS ASSOCIATED WITH THE ANALOG TO DIGITAL (A/D) CONVERSION CIRCUITRY

The A/D converter errors are attributable to the following sources: (1) errors in reference voltage. (2) errors in comparator threshold, (3) offset errors and gain errors in the operational amplifier used in the A/D converter. (4) errors in the feedback resistors used in the A/D converter operational amplifier. (5) quantizing errors, and (6) errors caused by leakage or by "on" resistance in the Fet transistor switches used in the A/D converter board and in the commutating input gates.

a. Reference Voltage Errors

The circuit which is used to generate the +2.500V and the -2.500V reference voltages for the A/D converter is shown in Figure 16a. An explanation of the operation of this circuit is given in Section III. The equivalent circuit of the reference circuit is shown in Figure 16b. The error voltage ΔE_1 which results from the worst case combination of variations in E_z with temperature, variations in R19 with temperature, and variations in the +15 volt source (ΔE_b) with temperature is given by

$$\Delta E_1 \approx R_z \left(\frac{\Delta E_b}{R19} + \frac{E_b - E_z}{R19} \cdot \frac{\Delta R19}{R19} \right) + \frac{\partial E_z}{\partial T} \Delta T$$

The 15V power supply, E_b, has been designed to be accurate over temperature to a tolerance of $\pm$ 1/2 percent; therefore, ΔE_b = 0.075. Resistor R19 has a temperature coefficient of 100 ppm and thus will change by $\pm$ 0.3 percent over temperature, i.e.

$$\frac{\Delta R19}{R19} = 0.003.$$

Using the above values of ΔE_b and $\Delta R19/R19$ and also using the parameter values given in Figure 16b for D7, R19, and using $\Delta T = \pm 30^{\circ}C$, one obtains

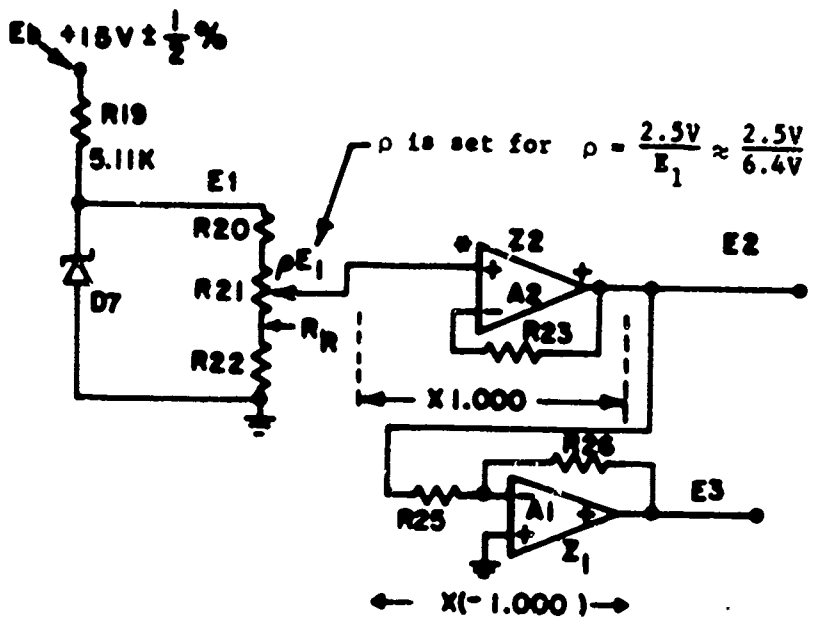
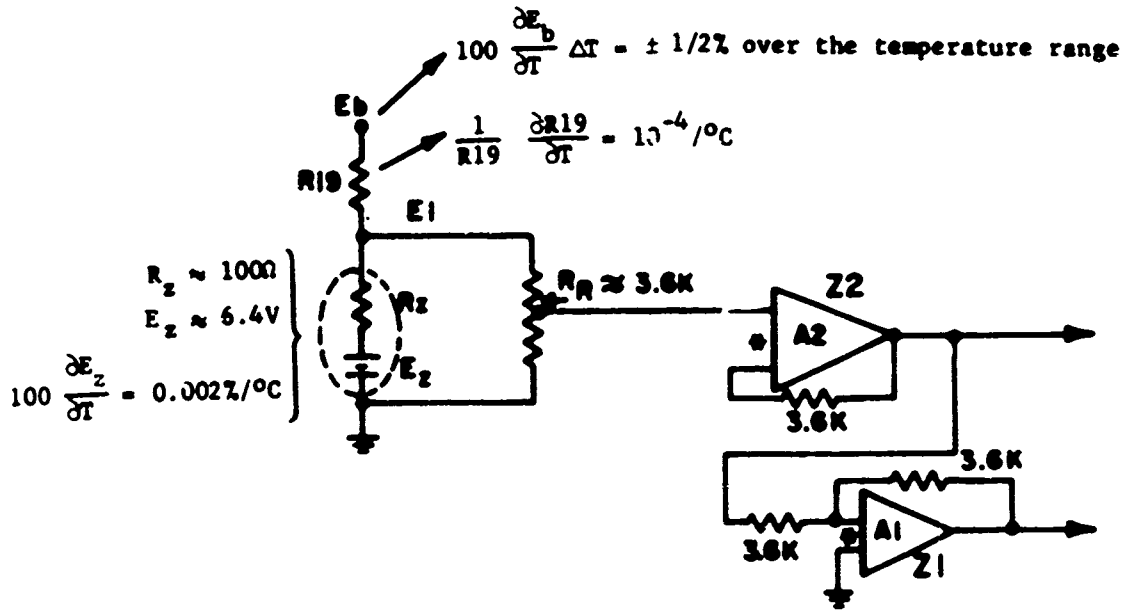


Figure 16a. Reference circuit.



*Definitions of operational amplifier input characteristics:

I_+ = bias current into non-inverting input

I_- = bias current into inverting input

E_{offset} = input voltage offset

$\frac{\partial E_{offset}}{\partial T}$ = temperature coefficient of offset = 0.003mV/°C for A1 and A2

$I_{offset} = (I_+)-(I_-)$ = input current offset

$\frac{\partial I_{offset}}{\partial T}$ = temperature coefficient of offset ≈ 2 na/°C for A1 and A2.

Temperature coefficient of either I_+ or I_- ≈ 6.25 na/°C

Figure 16b. Equivalent circuit of Figure 16a.

$$\Delta E_1 = \pm 100 \left(\frac{0.075}{5110} + \frac{15-6.4}{5110} \times 0.003 \right) + \frac{0.002}{100} \times 30 \times 6.4V$$

$$\Delta E_1 = \pm 5.81 \text{ millivolts (max.)}$$

The error voltage which is present at the input to A2 is given by ΔE_1 and is equal to 2.5/6.4 x 5.81 mV = 2.27 mV. The error voltage, ΔE_2, present at the output of Z2 is given by

$$\Delta E_2 = \Delta\Delta E_1 + \frac{\partial E_{offset}}{\partial T} \Delta T + \left[R23 \frac{\partial I_+}{\partial T} - R_R \frac{\partial I_-}{\partial T} \right] \Delta T$$

However, because of the selection of R20, R21, and R22 in the design, R_R will be equal to R23 and ΔE_2 simplifies to

$$\Delta E_2 = \Delta\Delta E_1 + \frac{\partial E_{offset}}{\partial T} \Delta T + R23 \frac{\partial I_{offset}}{\partial T} \Delta T$$

Using values of $\frac{\partial E_{offset}}{\partial T}$ and $\frac{\partial I_{offset}}{\partial T}$ given in Figure 12b, one obtains

$$\Delta E_2 = 2.27 \text{ mV} + [0.003 + 3600 \times 2.0 \times 10^{-6}] \ 30 \text{ mV}$$

$$\Delta E_2 = 2.58 \text{ mV (max.)}$$

The error voltage, ΔE_3, at the output of A1 is given by

$$\Delta E_3 \approx |-\Delta E_2| + \left[\frac{R26 + R25}{R25} \frac{\partial E_{offset}}{\partial T} + \frac{\partial I_-}{\partial T} R26 \right] \Delta T$$

Substituting the values shown in Figure 16 for the components gives

$$\Delta E_3 \approx 2.58 + (2 \times 0.003 + 6.25 \times 10^{-6} \times 3600) \ 30 \text{ millivolts}$$

$$\Delta E_3 = \pm 3.44 \text{ millivolts (max.)}$$

The effect of errors caused by changes in R25, R26, R20, and R22 has been neglected. These resistors are wirewound and have temperature coefficients which are matched to less than 10 ppm/^{o}C. Therefore, for $\pm 30^{o}$ change, the maximum change experienced by one of these resistors would only be 0.03 percent.

b. Comparator Error

The error introduced by the comparator (Z3 in Figure 8) in the A/D converter is similar to the error introduced by Z2 (in Figure 9) with the

exception that the effects of input bias current can be neglected because of the low output impedance of the input signals to Z3. Thus, the comparator error is given by

$$\Delta E_C = \frac{\partial E_{offset}}{\partial T} \Delta T = 0.003\ mV/^oC \times 30^oC = 0.09\ millivolt$$

c. Errors Related to Operational Amplifier

The errors resulting from the operational amplifier in the A/D converter will be primarily those introduced by the effects of changes in feedback resistance values R9, R19, and R18, effects of finite amplifier gain, A, and the effects of input offset voltage. The effects of input impedance and input bias current are negligible because field effect transistors are used for the input stage. The operational amplifier consists of input stage Q15-Q16 (also Q13-Q14 or Q11-Q12 depending on which pair is in the active condition) followed by intermediate stages Q3, Q4, Q5, and Q6. The output stage, Q7 is an emitter follower stage and is used to provide a low output impedance.

The output voltage, e_2, of the operational amplifier at the emitter of Q7 is related to the inverting input e_1 (at the drains of Q34 and Q8 and the non-inverting input e_{n1} (this will be either the voltage at pin 28, across C1 or across C2, depending on input pair selected) in the following manner:

$$e_2 = \frac{\left[(e_{ni} + e_{offset})\left(1 + \frac{R9 + R19}{R18}\right) - e_1 \frac{R9 + R19}{R18}\right]}{1 + \frac{1}{A}\left(1 + \frac{R9 + R19}{R18}\right)}$$

In the above equations, A is the amplifier gain and resistors R18, R19, and R9 are the precision feedback resistors identified in Figure 8 and e_{offset} represents the input offset voltage of the selected input stage. For the condition R9 + R19 $\approx$ R18, the errors introduced in e_2 (neglecting second order terms) will be:

$$\Delta e_2 \approx 2 \frac{\partial e_{offset}}{\partial T} \Delta T + 2 \frac{e_2}{A} \cdot \frac{\Delta A}{A} + (e_2 - e_{ni}) \left[\frac{\Delta(R9+R19)}{R9+R19} - \frac{\Delta R18}{R18}\right]$$

Maximum error occurs at $e_{ni} = 0V$, $e_2 = e_2|_{max} = 5.0V$, $A = A|_{min}$, and $\Delta A/A = \Delta A/A|_{max}$.

The maximum value of $\partial e_{offset}/\partial T$ for the UC 2132 transistor used in the input stage is given the value of $20 \times 10^{-6} V/^oC$ by the manufacturer. By design, A_{min} is 3000 and $\Delta A/A_{max} \approx \pm 0.3$ over the $\pm 30^oC$ expected temperature range. As a result of the 10 ppm temperature match for R19 and R18, the term

$$\left[\frac{(R9 + R19)}{R9 + R19} - \frac{R18}{R18}\right]_{max} \quad 10^{-5}/^{\circ}C \times 30^{\circ}C \quad 3 \times 10^{-4}$$

Using these values in the equation for e_2 max yields:

$$e_2 \quad 20 \times 10^{-6} \times 30 \times 2 + \frac{2 \times 5.0}{3000} \times 0.3 + 3 \times 10^{-4} \times 5.0$$

$$e_2 \quad 3.7 \text{ millivolts (max.)}$$

An actual temperature test has been performed on a breadboard version of the operational amplifier used in the prototype system. For operation over a temperature range of -11°C to +51°C, the peak value of error observed at the output of the amplifier was 1.0 mV, thereby tending to confirm the validity of the above analysis.

d. Quantizing Errors

Quantizing errors in the system can be neglected since a 14-bit resolution is used for the A/D converter even though the basic system accuracy is designed to a 0.1 percent tolerance.

e. Fet Switch Errors

Errors introduced by the Fet transistors are usually associated with either finite "on" resistance or with leakage currents. Errors attributable to "on" resistance effects are associated with the electronic switches used in the system. Switch transistors Q34 and Q8 in Figure 8 illustrate the effects of "on" resistance. These transistors are used to switch feedback resistor R18 to either the -2.500 V reference or to the +2.500 V reference. Because the "on" resistance of either Q34 or Q8 will be in series with R18, the effective value of R18 will be increased by R_{on}. the on resistance value. At a given temperature, the increase represents a fixed amount which usually is trimmed out at room temperature during final test. However, under temperature variations, R_{on} (of Q8 and Q34) will vary so that the amplifier gain will change by the following percentage:

$$\text{percentage gain change} \quad 100 \frac{R_{on}}{R_{on} + R18} \cdot \frac{1}{R_{on}} \left(\frac{\Delta R_{on}}{\Delta T}\right) \Delta T$$

Using a conservative value of 0.66 percent/°C for $\frac{100}{R_{on}} \frac{\Delta R_{on}}{\Delta T}$, a $\pm$ 30°C value for ΔT and R_{on} 60 Ω (max values for 2N4860) one obtains:

$$\text{percentage gain change} \quad \frac{60 \times 0.66 \times 30}{45,000 + 60} = \pm 0.026$$

Thus, error effects from this source will be neglected. Errors resulting from leakage currents in the Fet switch transistors will dominate only at high temperatures. In the case of the 2N3824 used in the commutating input gases, the room temperature maximum drain leakage figure is of $I_{d\ off} = 0.1$ nanoamperes but will increase by a factor of 2^4 at 65°C. Therefore, a maximum value of 1.6 nanoamperes represents a conservative figure to use for computing perturbation effects resulting from $I_{d\ off\ (max)}$.

The seven commutating gates which are used to switch the selected input signal to the A/D converter are shown in Figure 7. At any particular time, six of these gates are "off" and thus contribute a maximum leakage current of $6 \times I_{d\ off\ (max)}$ 6 x 1.6 9.6 nanoamperes to the input circuit. The seventh gate represents the selected channel which, in the case of one of the accelerometer channels, will have an output impedance of 15,000 ohms as a result of the R-C low pass filter at the output of each accelerometer.

The maximum error voltage which will appear at the input of the A/D converter will thus be:

$$e = 6\ I_{d\ off\ (max)}\ R_{out} = 9.6 \times 10^{-9} \times 15.000\ \Omega$$

$$e = 145\ \mu V$$

This is obviously insignificant since it represents an error less than a 0.01 percent of full scale.

Another possible source of error results from charge removal from "hold" condenser C1 (and C2). This will occur at a rate proportional to the leakage currents in the gate of Q11 (Q14) and in the drain of Q25 (Q28). The total voltages error produced will depend on the length of the "hold" interval, ΔT, and will be in the form

$$e_i = \frac{I_{leakage}\ \Delta T}{C1}$$

The maximum gate leakage for the Q11 is (by coincidence) the same as $I_{d\ off\ (max)}$ for Q25; therefore, $I_{leakage}$ will have a total value of $(1.6 + 1.6) = 3.2 \times 10^{-9}$ amperes. Condenser C1 has a value of 5100×10^{-12} farads. The value of ΔT will be 667×10^{-6} seconds if ΔT is taken to represent a worst case condition of two complete bit periods. Therefore, the maximum value of e_i will be:

$$e_{i\ max} = \frac{3.2 \times 10^{-9} \times 667 \times 10^{-6}}{5100 \times 10 - 12}$$

$$= 0.418\ \text{millivolts}$$

This error is less than 0.02 percent of full scale and will therefore be ignored.

Additional sources of error such as those caused by noise pulses generated by the switching action of the logic circuitry were taken into consideration during the design phase and during the layout of the prototype system. As a further precaution. noise pulses generated by the logic circuitry have been held to very low levels by making use of very low power integrated circuitry for the logic elements.

3. TEST RESULTS

A series of tests were performed on the prototype probe system to confirm the accuracy of the system's design at room temperature and also at elevated and reduced temperatures. For these tests, the X axis accelerometer output was temporarily disconnected and a precision reference source was used as the input. The digital output of the system was recorded for each input voltage. At the end of the test. an analog equivalent was computed from the digital output and then compared with the input voltage. The results of these measurements are summarized in Table 2. It can be seen that for temperatures between -6°C and +60°C, the offset can be expected to hold within ± 0.1 percent of full scale. The scale factor varied by less than ± 0.02 percent for the same range of temperatures.

During the tests transmitter power was monitored and found to vary from a value of 100 milliwatts at -6°C to a maximum of 150 milliwatts a room temperature. The transmitter frequency varied from a low value of 1694 MHz at 60°C to 1700 MHz at 27°C.

The prototype system can be operated with external power as well as with its normal power source consisting of a rechargeable nickel-cadmium battery pack. The use of external power is useful during tests because of the limited operating time provided by the battery pack. When powered on its internal battery pack alone. the prototype system will operate for a minimum of 40 minutes if the batteries are at a fully-charged condition at the start of the test.

A battery pack using primary non-rechargeable alkaline batteries has also been used to operate the system. The substitute battery pack consisted of two series strings of Mallory Duracell batteries. type MN1500. Each string was composed of eight cells in series and the two strings were tied together in parallel to operate the prototype system. Using this arrangement. an operating time of 40 minutes was obtained.

The shelf life capability of the MN1500 alkaline battery is excellent. The manufacturer claims retention of 80 percent of original battery capacity at the end of two years.

TABLE 2

RESULTS OF MEASUREMENTS ON PROTOTYPE PROBE SYSTEM USING PRECISION VOLTAGE SOURCE IN PLACE OF NORMAL X AXIS ACCELEROMETER INPUT

PARAMETER		DIGITAL OUTPUT CODE REPRESENTATION	TEMPERATURE			MEASUREMENT PROCEDURE
			140°F (60°C)	80°F (27°C)	22°F (-5.6°C)	
Scale factor		111111111111XX for positive full scale and 000000000000XX for negative full scale	4.994V	4.9934V	4.9928V	Algebraic difference between positive full scale input voltage and negative full scale input voltages ($V_{max} - V_{min}$)
Midrange error (zero offset)		011111111111XX or 100000000000XX	-5.0 mV	-1.5 mV	+2.0 mV	One half of algebraic sum of positive full scale input voltage and negative full scale input voltage $1/2(V_{max} - V_{min})$
Nonlinearity errors	1/4 full scale (≈ -1.25V)	001111111111XX or 010000000000XX	0.7 ± 0.2 mV	1.1 ± 0.5 mV	0.1 ± 1.5 mV	Departure of input voltage from value predicted by straight line drawn between positive full scale input voltage and negative full scale input voltage
	Midrange (≈ 0 V)	011111111111XX or 100000000000XX	0.55 ± 0.005 mV	0 ± 0.7 mV	0.1 ± 0.4 mV	
	3/4 full scale (≈ +1.25V)	101111111111XX or 110000000000XX	0.9 ± 0.15 mV	0.25 ± 0.7 mV	0.3 ± 1.4 mV	

SECTION VII

GROUND STATION SYSTEM

1. SYSTEM DESCRIPTION AND OPERATION

The system of Figure 17 shown in block diagram form illustrates the method by which the digital data is processed by the ground station. Figure 18 shows the decoder circuits portion of the portable ground station system in more detailed form. Basically the system provides a direct recording of the raw data appearing at the output of the GMD-1 FM detector, a three-channel analog output signal representing the three axes of acceleration, and an operator selected analog output representing either A_x, A_y, A_z, T_x, T_y, or T_z data. This latter output may be applied either to a digital voltmeter for a numerical readout or to an oscilloscope for waveform observation. A detailed description of the ground station electronics is given below.

2. TAPE RECORDING CIRCUITS

In order to minimize the possibility of data loss caused by ground station equipment malfunction, the GMD-1 output data in subcarrier form is directly recorded on Channel No. 1 of the seven channel ampex model FR1300 analog tape recorder shown in the figure. Channel No. 2 is used for audio recordings and is provided in order to allow operator commentary during key phases of the flight, e.g., launch, tracking acquisition, payload separation, etc. A time reference for the recording is provided using one of the irig time code inputs which are available at launch sites and recording this on Channel No. 3 of the tape recorder. The remaining four channels are available to allow for system expansion at a future date.

3. TRANSLATION CIRCUITS

In order to insure proper decoding of the telemetered signal, it is necessary that proper synchronization be maintained between the circuitry in the falling sphere and the ground station circuits. This is accomplished by successively passing the output signal of the GMD-1 receiver through a subcarrier discriminator, a sync filter and a sync bit detector circuit. The output pulses on the sync bit detector are applied to the sync code decoder consisting of storage register SR1 (modules A7, A10, A11, and A12), a set of buffer amplifiers (A13), two comparators a7 and a8 (A14), an output gate, and two multivibrators MV1 and MV2. Register SR1 is a 20-stage shift register which is used for temporary storage of the five bits representing the sync code. It is advanced at a rate which is four times the system's bit rate, thereby permitting the determination of synchronization to a resolution of 1/4 of a bit interval. The outputs of the five equally spaced stages of SR1, which are used to detect the presence of the sync code, are applied to comparator a7 using the five summing resistors which are shown in

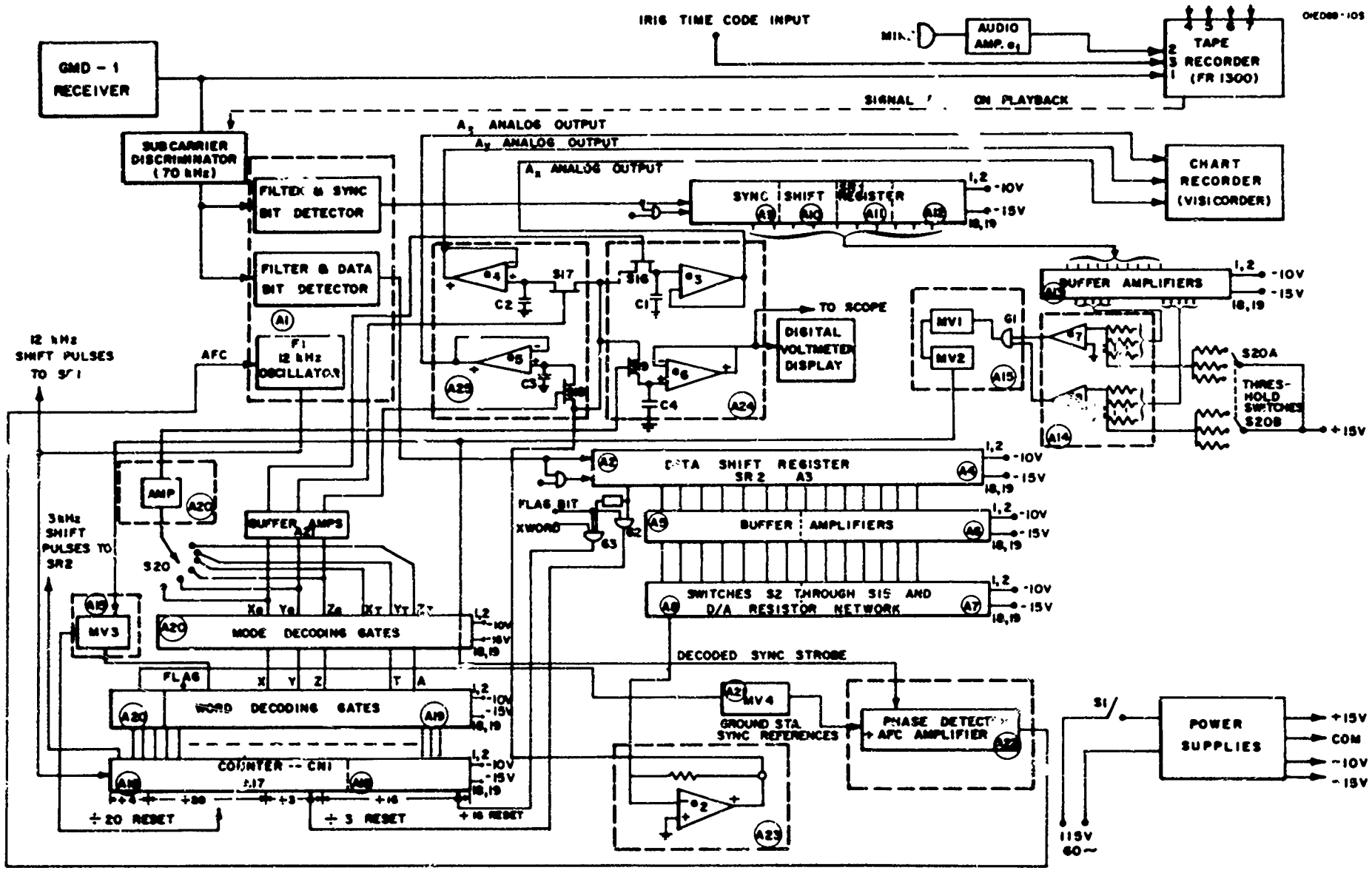


Figure 17. Ground station system block diagram.

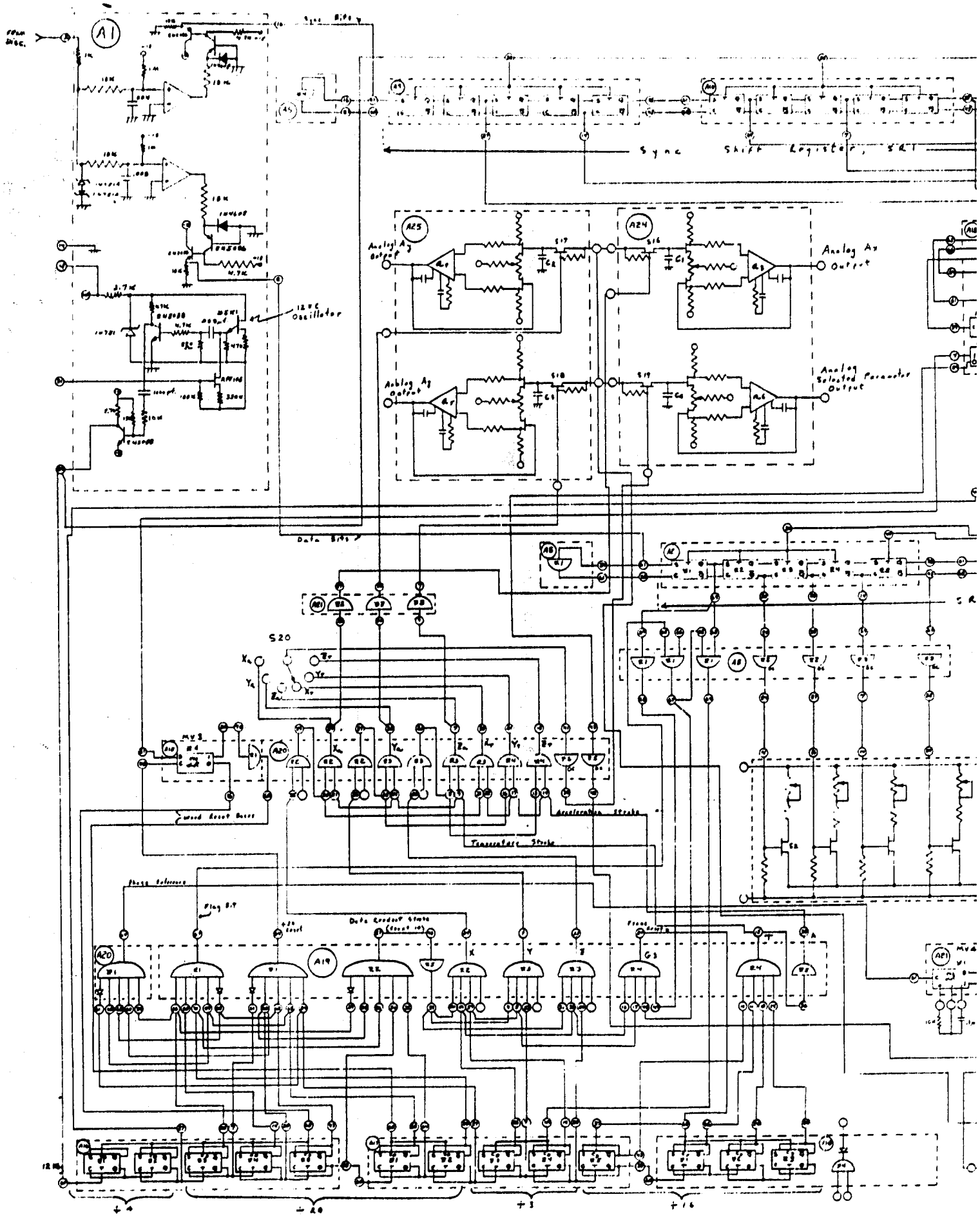
in the figure. Provision is made to invert the output of the stage representing the fourth bit of the sync code; thus, the sync code is converted from 11101 to 11111 at the input to a7. When all five bits of the sync code have been loaded into the proper positions in SR1, the threshold bias at the input to a7 is exceeded and an output of a7 is produced. A second comparator, a8, similar to a7 is used to sense for the "interpulse" zero condition which for a properly transmitted sync signal has to be present during an output condition of a7. This characteristic follows as a direct consequence of the return to zero (RZ) format used for the sync code.

The coincidence condition of an output from a7 plus a simultaneous output from a8 is sensed by gate G1 which is used to turn on MV1 and MV2. The output of MV2 clears the divide by 20 and the divide by 4 stages in counter CN1 thereby establishing the proper starting point for decoding the data bits which immediately follow.

Because each telemetered word of data is prefixed by the sync code, a synchronizing output signal is available at a once-per-word rate (150 pps). Therefore, loss of synchronization should not be a problem. In order to maintain synchronization during the interval between sync codes, the output of a phase locked 12 kHz frequency oscillator, F1, is counted in counter CN1. The outputs of CN1 consists of a series of time-strobe pulses which are used to properly decode the incoming signals. In normal operation, the divide by 20 output of CN1 represents the word sync reference and should occur in time coincidence with the output of the sync code detector. A phase detector checks for this coincidence using the output of MV2 and the output of MV4. If a departure from coincidence is present, the phase detector output will produce an AFC feedback voltage which will cause the frequency and phase of F1 to shift by the amount and in the direction required to essentially achieve a coincidence condition.

The 15 bits of digital data which follow the sync code represent a flag bit, 10 bits of useful digital data, and four data bits of less precise data. The digital data is filtered, detected, and applied to the 15 bit data shift register, SR2. The data shift register is advanced by the divide of 4 output of the CN1 at the required bit rate of 3 kHz. When the flag bit has been shifted into the first stage of SR2, an output strobe is applied both to G2, in order to check the X flag bit for word synchronization and to G3, which senses the X flag bit for the frame reference point (temperature interval). After synchronization is established a one state of the X flag bit indicates an acceleration readout while a zero state of the X flag indicates a temperature readout. After an interval of 14 bits after the flag bit has been examined, a separate readout pulse representing either the X, Y, and Z strobe (depending on word phase) is applied to S16, S17, S18 in order to read out acceleration data.

At the end of each shift operation of SR2, an analog current is delivered to operational amplifier, a2, by means of a set of weighted resistors in modules A7 and A8. The resistors are connected to a reference voltage, E ref., through a set of switches, S2 to S15, which are either



* Note: Gates in these modules have open collector (OC) outputs. See data sheets for Pin and Internal Circuit

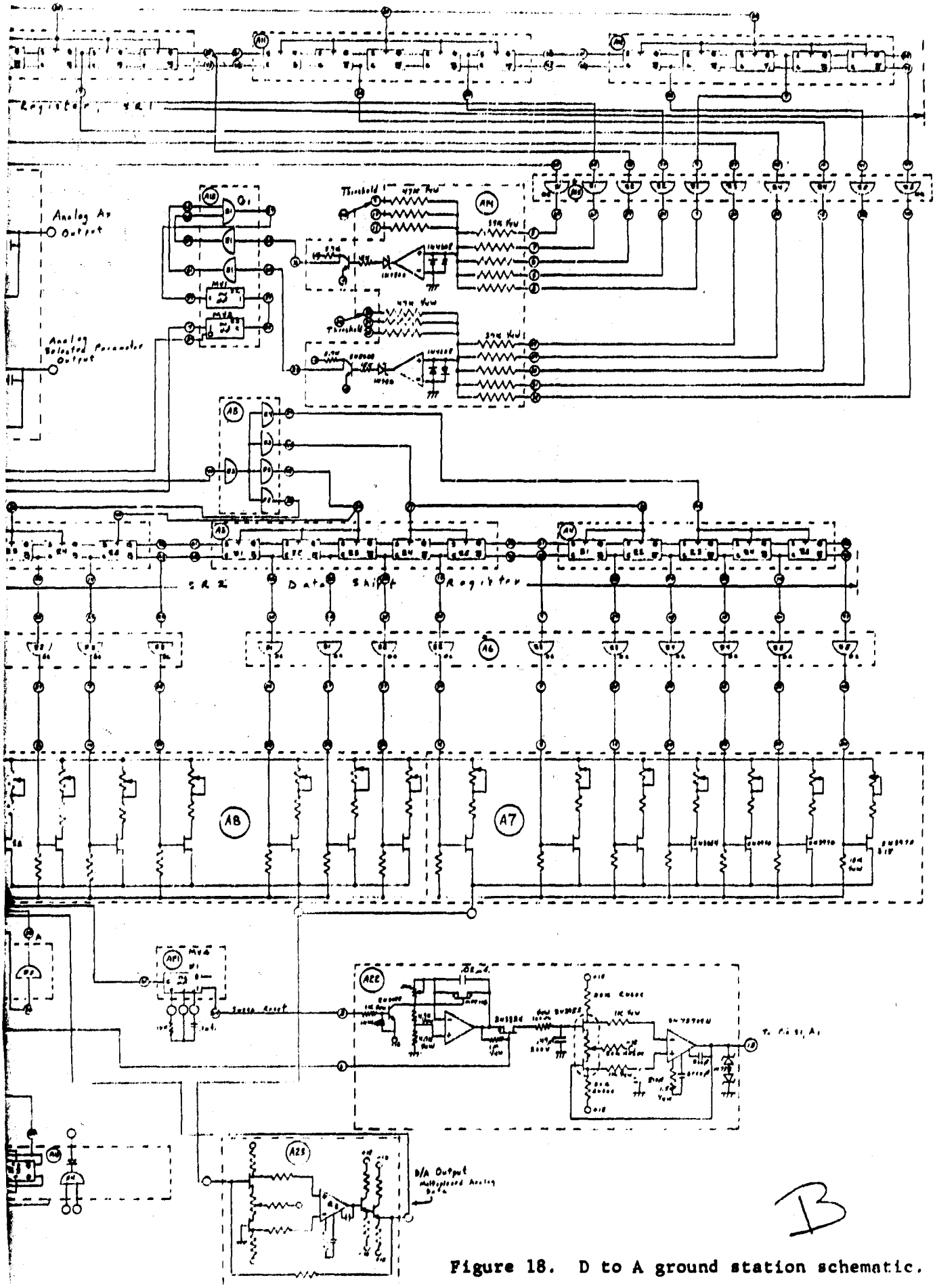


Figure 18. D to A ground station schematic.

opened or closed in accordance with the data stored in each corresponding stage in SR2. Until all 15 bits of data have been entered into SR2, the output voltage of a2 does not represent a meaningful signal and is therefore ignored. However, at the times of which the X, Y, or Z strobes occur, the output of a2 represents the voltage analog of the acceleration components A_X, A_Y, or A_Z, respectively. Using the appropriate strobes, these analog outputs are switched into sample and hold amplifiers a3, a4, and a5 by means of S16, S17, and S18. Normally, A_X is read into a3 by the X strobe and held during the next two-word intervals which contain the Y and Z data bits. Similarly Y is read into a4 and held during the Z and X intervals. As a result of the time multiplexing of the A_X, A_Y, and A_Z data, the data rate for each axis will be one-third of the basic 150 wps word rate or 50 acceleration readings per second. The 150-pps word rate results from the 3-kHz bit rate and 20-bit word format (5 bits for sync and 15 bits for data). In addition to the acceleration data, temperature data from three temperature sensors is transmitted in place of the acceleration data once in every 16 cycles of data, giving a data frame rate of approximately 50/16 = 3-1/8 pps. During the temperature interval, a read-in into a3, a4, and a5 will not take place in order to avoid contaminating the acceleration data with temperature data. Instead the outputs of a3, a4, and a5 will be held at their previous values. Proper synchronization of the temperature readout is accomplished at a 3-1/8 pps rate by the output of G3.

4. SELECTED ANALOG CHANNEL

Sample and hold amplifier a6 is used to present either A_X, A_Y, A_Z, T_X, T_Y, or T_Z to an output circuit in accordance with the position of selector switch S20. The method of operation is similar to that described above for a3, a4, and a5. The selection of output parameter is accomplished using the word and mode (frame) decoding gates in modules A19 and A20 in conjunction with the outputs of CN1 and selector switch S20. The output of a6 is especially useful during the calibration of the accelerometer in a finished system. The axis to be calibrated can be selected by S20 and a digital voltmeter may be connected to the output of a6 to provide a precise readout.

SECTION VIII

RECOMMENDATIONS

1. AIRBORNE UNIT

a. Prototype Unit

Because of the developmental nature of the probe design, the circuit boards containing the signal processing electronics have been fabricated using hand-wired circuitry so that circuit alterations and improvements could readily be accommodated. Because of high component density, the use of hand wiring and the extensive testing, the prototype unit cannot be expected to survive as high an environmental stress such as vibration and shock as will be possible in the case of future production units. However, in order to harden the prototype unit for possible flight, a complete inspection of the prototype unit was performed at the conclusion of the test program. The critical circuit elements, which were found to be particularly vulnerable to environmental stresses, have been suitably reinforced. Consequently, it is the opinion of GCA that the prototype unit can withstand the rigors of launch. GCA, therefore, recommends that the routine shock and vibration test be performed on the prototype probe unit; and upon sucessful completion of the tests, the unit be flown.

b. Future Improvements

Two avenues of approach are available in future systems for increasing the dynamic range of the measurement. One approach would be to directly improve system accuracy by taking steps to reduce the error contributions discussed in Section VI. Because the system already provides for a 14-bit resolution, no extensive redesign is required to improve system accuracy. It is anticipated that most of the improvement can be obtained simply by direct substitution of more precise components in place of the existing components. For example, reference diodes, operational amplifiers, and precision resistors having lower temperature coefficients than those used in the prototype unit are available.

The second avenue of approach would be the use of a two channel dual-gain processing system for the outputs of each accelerometer. The signal level in one channel would be the same as in the present system and would represent the low sensitivity output. The signal level in the other channel would have a gain of approximately 20 and would constitute the high sensitivity output.

Of the two approaches for system improvement, the improved accuracy 14-bit system would be less complex but would require much more attention to the details of design and layout.

The PCM code utilized in the prototype system employs a return to zero (RZ) format for the synchronizing portion but not for the data portion. This results in an improvement in signal-to-noise ratio for the data. However, if data reduction facilities with which the system is to be used cannot accommodate the non return to zero (NRZ) format, a very simple wiring change (one wire) will allow the modification of the system to the RZ format for both data and synchronization.

Although the nickel-cadmium system proved to be a convenience in the prototype system because of its recharging feature, this may not prove to be desirable for a production type system intended for field use with non-skilled operators. The battery requirements of a production probe system have been evaluated and the characteristics of non-rechargeable batteries such as the alkaline and mercury types have been reviewed. Both types have good shelf life but the mercury type cannot meet the high discharge rate required by the probe circuitry. Tests using the alkaline cells are described in Section VI and indicate satisfactory performance. Furthermore, their very low cost ($0.33 per cell) makes the alkaline-battery system attractive from an economic point of view.

2. MECHANICAL DESIGN

a. Nose Cone

Investigation should be made to use a fiberglass reinforced plastic material for the split nose cone. The primary objective of this should be to mold the two halves of the nose cone to the final dimensions thus obviating machining operations and reducing production costs. Thickness of the shell should be about 0.2 inch.

Note that use of a fiberglass shell also allows the option of turning the transmitter on before sphere ejection.

b. Release Mechanism

The parts of the release mechanism are simple and lend themselves to being cast rather than machined. This includes the split ring.

c. Pyrotechnic Circuit

Presently the material cost of the pyrotechnic circuit is about $250. This cost can be reduced by investigating less expensive timers, batteries, and barometric switch. For example, the present barometric switch cost $40 whereas other units now available are about $5.

d. Strut

The parts for the inflation system (cylinder and piston) and the

accelerometer mount can be made from castings and finish machined to reduce costs. Also the nylon housing for the transmitter can be finish-molded plastic, thus avoiding machining costs.

In general, one may conclude that with respect to the mechanical design of the system, production manufacturing methods can be used for cost advantages. The existing provision to recharge the instrumentation batteries externally, when the nose cone is fully assembled, simplifies operational use of the inflatable sphere as a practical meteorological density measurement system.

SECTION IX

DRAWING LIST

SKC105864	VOLTAGE REGULATOR AND REF. SUPPLY
SKC105865	A TO D CONVERTER
SKC105866	POWER SUPPLY
SKE105867	LAYOUT A TO D
SKE105872	POWER WIRING LOGIC CIRCUIT
SKE105873	SIGNAL WIRING LOGIC CIRCUIT
SKC105910	SCHEMATIC LOGIC CIRCUIT
SKE105911	LAYOUT BREADBOARD LOGIC CIRCUIT
SKD105912	PC MASTER LOGIC CIRCUIT
SKC105916	SCHEMATIC COMMUTATING INPUT GATES
SKE105917	LAYOUT COMMUTATING INPUT GATES
SKD105918	PC MASTER COMMUTATING INPUT GATES
SKD105920	PC MASTER A TO D CONVERTER
E105926	PC MASTER DC TO DC CONVERTER
E105927	MACHINE PC DC TO DC CONVERTER
SKD105928	SCHEMATIC 70 KC VCO
SKE105929	LAYOUT VCO AND POWER SUPPLY
A105934	PARTS LIST FOR DC TO DC CONVERTER
A105935	PARTS LIST FOR A TO D CONVERTER
A105936	PARTS LIST FOR COMMUTATING GATES
A105938	PARTS LIST FOR 70 KC VCO AND REGULATORS
C105939	HOUSING - ELECTRONICS
C105940	COUPLING RING
C105941	CARD SUPPORT
B105942	CONNECTOR PLATE
B105943	GASKET
B105944	SPACER
B105945	CARD PLATE BOTTOM
C105946	CYLINDER INFLATION
B105947	COVER AFT END
SKC105948	CARD INTERWIRING
B105950	PISTON
B105951	POST
B105952	WASHER
B105953	GASKET #1
B105954	RETAINER AFT END
SKB105955	SYSTEM WIRING
E105956	PC MASTER VOC AND POWER SUPPLY
D105957	MOUNT ACCELEROMETER
B105959	INSULATOR BOARD
C105960	BATTERY PLATE
B105961	ALIGNMENT TAB
C105962	BATTERY PLATE #2
C105963	BATTERY PLATE #3
B105964	SUPPORT BRKT
C105965	RELEASE BLOCK FIXED
C105967	RELEASE BLOCK MOVABLE
B105968	RETENTION ROD
B105969	GROUND SLEEVE

C105970	SPLIT RING
D105975	COUPLING RING
B105977	CAPACITOR
B105978	SLEEVE
B105979	STRAP
D105981	PC MASTER A TO D CONVERTER #2
D106003	A TO D MACHINE PRINT #2
D106005	A TO D WIRING DIAG. #2
B106027	UPPER COUPLING RING
C106028	ANTENNA HOUSING
C106095	TRANSMITTER BRACKET
E106105	D TO A GROUND STATION SCHEMATIC
E106160	DC TO DC CONVERTER ASSEMBLY

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13 ABSTRACT

Under contract F19628-67-C-0218, GCA Corporation has completed the design for a rocket probe system which will determine air density at altitudes of 70 to 130 km. The GCA design differes from that of similar probes presently being used for obtaining density measurements primarily in the signal processing electronics. The GCA design employs a digital processor which encodes 50 complete acceleration readings per second and generates a PCM output signal whereas previous probes have been analog in nature and have made use either of a multisubcarrier FM-FM system or a commutated signal subcarrier FM-FM system. In order to confirm the validity of the electrical design, a prototype unit has been fabricated and bench tested. Temperature tests have been performed on the prototype unit and indicates that over a 0 to +60°C temperature range, an accuracy figure of ±0.1 percent has been achieved for the signal processing electronics portion of the probe system. This represents an order of magnitude improvement in accuracy over a typical FM-FM system, thus fulfilling the initial accuracy of objectives of the program. Power for the system is supplied by an internal battery pack consisting of seven rechargeable nickel-cadmium cells which have a capacity sufficient to operate the probe system for a duration of 40 minutes at room temperature.

DD FORM 1 NOV 68 1473 REPLACES DD FORM 1473, 1 JAN 65.

14. KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Sounding Rocket						
Sparrow Arcas						
Atmospheric Density						
Accelerometer						
Falling Sphere						
A/D Conversion						
Telemeter						